**ECE 209: Logic and Computing Devices Lab**

**Clemson University**

**Fall 20\*\***

**Section 001: 8:00 – 10:00 AM Tuesday**

**Instructor Name:** TA Name

**Email:** \*\*\*@clemson.edu

**Office Hours:** Please email to arrange an appointment

**Lab Location:**  Riggs 322

**Lab Coordinator:**

Name: Dr. Timothy Burg

Email: tburg@clemson.edu

Office: 307 Fluor Daniel (EIB)

Phone: 864-656-1368

**Lab Homepage:**

[**http://www.clemson.edu/ces/departments/ece/resources/ECE209Lab.html**](http://www.clemson.edu/ces/departments/ece/resources/ECE209Lab.html)

**Objective:**

To develop the knowledge to design and analyze combinational and sequential circuits. This laboratory primarily aims to reinforce the concepts introduced in ECE 201.

**Required Materials:** 209 Lab Kit, NI ELVIS II, Lab Manual, Digital Works software,

* **209 Lab Kit:** You should have obtained the kit prior to lab 1. Lab kit notes are included in the ECE 209 lab manual available on the lab homepage.
* **NI ELVIS II:** You will be using the NI ELVIS II kit to perform your experiments. Manual to this equipment is included in the ECE 209 lab manual.
* **Lab Manual:** The ECE 209 lab manual is to be downloaded from the link mentioned above. You will have to bring this lab manual to lab.
* **Digital Works Software:** The software along with its manual and required macros can be obtained from the lab homepage. Students using 64 bit machines can download the software from <http://www.electronics-lab.com/downloads/schematic/002/index.html>

**Grading:**

25% Pre-Lab preparation and design

25% Class performance and demonstration of functional circuits

30% Full lab reports

20% Final project and presentation

**Tentative Grading Scale:**

A: 90-100%

B: 75-89%

C: 60-74%

D: 50-59%

F: <50%

**Attendance:**

Attendance is mandatory for every lab. If special circumstances arise that prevents the student from attending a lab session, he/she must notify the instructor at the earliest, and a makeup lab session will be given at the instructor’s discretion. If the instructor is not in the classroom within **15 minutes** after the class is scheduled to start, then unless told otherwise, students are free to leave.

**Pre-lab preparation and design:**

Much of the work required to successfully build a functional circuit should be completed by the student **before** starting the lab session.

* **Preparation:** You are expected to thoroughly read each lab experiment (available in the manual) prior to the lab session. This is extremely important to ensure timely completion of the experiment.
* **Pre-lab reports:** Each student must submit a brief pre-lab reportprior to starting the experiment. It may be either hand written or printed from a word processor. Please note that unless provided with a valid reason, the instructor reserves the right to reduce grades for late submission.
* **Pre-wire your circuits:** You are strongly encouraged to pre-wire the circuit on your breadboard to the maximum possible extent before coming to the lab. Otherwise you could risk not being able to complete the experiment in the assigned lab time, thus leading to possible reduction of grade. Proper preparation makes the lab fairly painless for both the students and instructor.

**Lab Reports:**

In addition to the brief lab reports to be submitted every week, the instructor will designate 3 lab experiments, for which you are expected to write detailed reports and submit by a scheduled date. These reports have to be typed using a word processor (or any other similar software) and printed out.

Note that:

* Diagrams, sketches and tables should be neat and must be labeled. Only computer drawn circuit diagrams will be accepted in these reports. Also, all logic equations must be clearly shown.
* Grade will be based on organization, content, neatness, accuracy, conclusions and format.
* Each report will consist of the following sections:

-Title page (Title, date, due date, author, lab partners)

-Objectives (State the purpose of the laboratory)

-Procedure, data (circuit diagrams) and results.

-Conclusion

-College of Engineering honor code.

-Signature of author

**Final Exam:** This course does not have a final exam.

**Final Project and presentation:**

The last component of this lab involves design, simulation and analysis of a digital-circuit or any related concept of your choice.

* You may work individually or in groups of 2.
* While simulation is not a requirement, make sure that the amount of time you spend is at least equivalent to 3 lab sessions per person (i.e. 6 hours).
* One report will have to be turned in for every group and a presentation will have to be made during the last lab session of the semester.
* Most importantly, this project is meant to be fun!! In the past, students have simulated numerous fun projects such as Basketball Scorecard simulation, Tic Tac Toe etc.

More information about this component of the course will be provided during the second half of the semester.

**Academic Integrity:**

Students are strongly encouraged to collaborate while performing experiments in the lab or while working on their final projects. However, all reports turned in must be the work of the student. All sources of help including websites, books, discussion with friends etc. must be clearly mentioned in the acknowledgment and reference sections of the report. All full lab reports and the final project report will have to be pledged as follows:

*“As members of the Clemson University community, we have inherited Thomas Green Clemson’s vision of this institution as a ‘high seminary of learning.’ Fundamental to this vision is a mutual commitment to truthfulness, honor, and responsibility, without which we cannot earn the trust and respect of others. Furthermore, we recognize that academic dishonesty detracts from the value of a Clemson degree. Therefore, we shall not tolerate lying, cheating, or stealing in any form.”*

*“When, in the opinion of a faculty member, there is evidence that a student has committed an act of academic dishonesty, the faculty member shall make a formal written charge of academic dishonesty, including a description of the misconduct, to the Associate Dean for Curriculum in the Office of Undergraduate Studies. At the same time, the faculty member may, but is not required to, inform each involved student privately of the nature of the alleged charge.”*

**Tentative Lab Schedule:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Week #** | **Date** | **Lab Title** | **Prelab** | **Full-lab** | **Simulation** | **Circuit Building** | **Other** |
| 0 | Sep 5 | Introduction | Not Reqd | Not Reqd | No | No |  |
| 1 | Sep 12 | Logic Gates | Sep 12 | Not Reqd | Yes | No |  |
| 2 | Sep 19 | Encoding/Decoding | Sep 19 | Oct 3 | Yes | Yes |  |
| 3 | Sep 26 | Combinational Circuits | Sep 26 | Not Reqd | Yes | Yes |  |
| 4 | Oct 3 | Binary Arithmetic | Oct 3 | Oct 24 | Yes | Yes |  |
| 5 | Oct 10 | MSI Circuits | Oct 10 | Not Reqd | Yes | Yes |  |
| 6 | Oct 17 | **FALL BREAK** |  |  |  |  |  |
| 7 | Oct 24 | Multipliers | Not Reqd | Not Reqd | Yes | No | Finalize project topic/team |
| 8 | Oct 31 | Multiplexers & Serial Comm. | Oct 31 | Nov 14 | Yes | Yes |  |
| 9 | Nov 7 | Memory Cache/Project | Not Reqd | Not Reqd | Yes | No |  |
| 10 | Nov 14 | Memory Cache/Project | Not Reqd | Not Reqd | Yes | No |  |
| 11 | Nov 21 | Sequential Design | Nov 21 | Not Reqd | Yes | Yes | Final project report due |
| **12** | **Nov 28** | **Final Project Presentation** |  |  |  |  | **PPT/Demo** |

**NOTE:** The instructor reserves the right to modify the syllabus as needed during the semester. Students will be notified prior to any changes.

\*Note: No lab the week of the Jan \*\* due to Martin Luther King Jr day

\*Note: No lab the week of the Nov \*\* due to Fall Break

\*Note: No lab the week of the Oct \*\* due to Thanksgiving Holiday