EE Laboratory IV - ECE 312

LABORATORY MANUAL

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ECE312 EE LABORATORY IV

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ECE 312 ELECTRICAL ENGINEERING LABORATORY IV

Introduction

A major goal of this set of laboratory projects is to is to put you as far as is possible in the position you may well find yourself as a future working electrical engineer. You will be required to complete a number of electronic system designs and be faced with difficulties and deadlines. Tools to help you in this process include a 350 MHz Pentium computer loaded with an evaluation copy of PSPICE and National Instruments LabView virtual instrumentation system with a DAQ board.

Design of any kind requires that you apply "up-front" effort to understand the system you are trying to design. With inadequate understanding you are often tempted to take a "try and hope " approach. With a small inexpensive system such as you will meet as a student this method sometimes works. However in the real world it may not be feasible due to project cost and complexity. In any case the "try and hope" approach is unprofessional and can lead you to make unsupportable technical decisions.

Even if you take the right approach by thinking and analysis, design may still be painful, time consuming and occasionally very frustrating. Sometimes you feel that Murphy is really out to get you whatever you do. However if, in spite of the barriers, you have devoted effort and your own creativity to solving a problem, the sense of accomplishment this brings can be one of the major rewards of being in this profession.

In this laboratory class you may experience some frustration as you cross swords with Mother Nature. However I hope also that you will gain a sense of accomplishment and a better understanding of the general design thought process which should be applicable to any design project you may be faced with in the future.

Michael A. Bridgwood

ELECTRICAL ENGINEERING LABORATORY IV

Schedule

Experiment 1	BJT Small signal parameters
Experiment 2	Operational Amplifiers
Experiment 3	Active Current Sources
Experiment 4	Differential Amplifers
Experiment 5	Sinusoidal Oscillators
Experiment 6	Level detection

EE LABORATORY IV

ECE 312

Experiment 1. BJT Small Signal Model Determination

PURPOSE:

This is an experimental session which uses knowledge gained in ECE 320 of bipolar transistors and at the same time provides an introduction to the use of the measurement station and LabView. The goal is a determination of the four parameters forming the hybrid or h parameter small signal model. Knowledge of these h parameters easily allows the hybrid π small signal parameters $r\pi$, gm and ro to be determined at a particular frequency.

EQUIPMENT REQUIRED:

1 CA3046 bipolar transistor array
1 CEU development station
3 2200 μF capacitors
Resistors as required

PROCEDURE

The parameters given in the following single stage BJT amplifier circuit using the CA3046 transistor array were the result of design aimed at setting the quiescent point at Ic = 1 mA and Vce = 3 volts. The nearest preferred resistance values are given in the circuit so that the quiescent point is not exactly at the values quoted. However it is near enough to be considered acceptable for most general purpose manufacturing requirements.

Part 1 Verify the design shown in Figure 1.1 theoretically and confirm the quiescent point position by measurement (Ic = 1mA, Vce = 3 volts).

Part 2 Determine values for hie and hfe at the quiescent point and at a frequency of 1 kHz.

Part 3 Determine values for hoe and hre at the same quiescent point and signal frequency.

Part 4 Share the values for hie and hfe which you obtain with other laboratory groups in your section. Determine the mean and standard deviation of each from the total data.

Check on values of hie and hfe by measuring overall voltage gain of circuit and compare with theoretical values.

Part 5. Write up this lab in the short form given in Appendix C. If you have difficulty obtaining any of the values comment on why you think this has occurred in your conclusions.

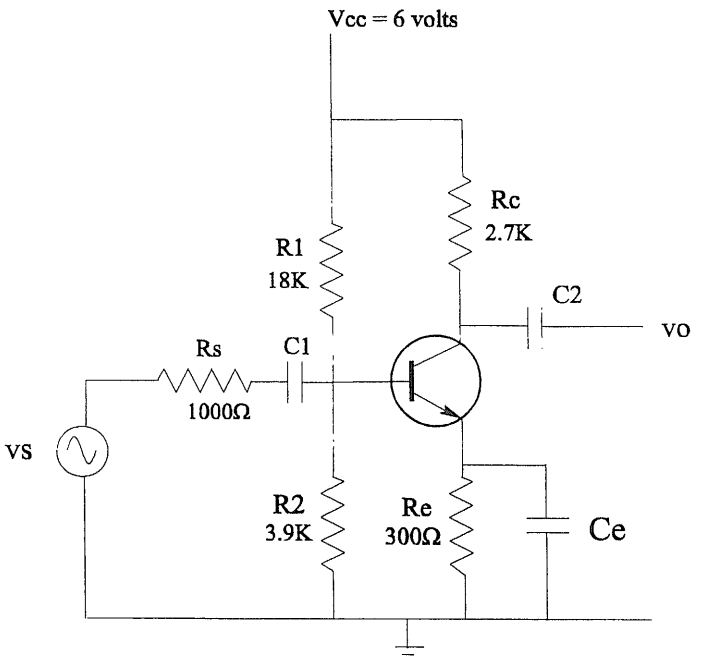

Figure 1.1 Single stage CE BJT amplifier

In order to determine hie, hfe, hfe and hoe by measurement, the circuit above requires "adjustment" so that the small signal model is configured in the right form to enable these small signal parameters to be extracted. (See theory section below).

Theory - h parameters and small signal model

In the theoretical support sections of this laboratory class most of the development of material involving BJT 's is written in terms of the h (hybrid) or reduced h parameter model in the common emitter mode since it is the model most often quoted in manufacturers' specifications. Hence this model will be examined in some detail.
The four parameters are identified in the full small signal h parameter model shown as Figure 1.2.

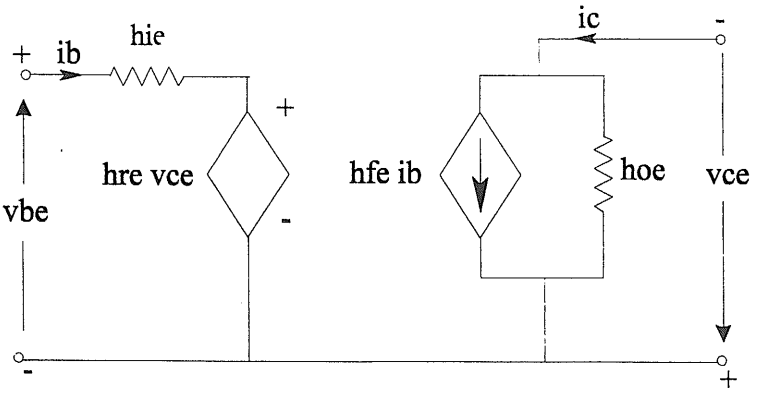

Figure 1.2 BJT small signal model for CE mode operation

The signs indicated in the above circuit represent the positive cycle of the small signal input vbe which is shown driving current ib through hie in the direction shown by the arrow in the base circuit. The arrow within the dependent source box hfeib indicates the direction that current is driven by the dependent source. This direction is directly linked to that of ib so that when the input voltage vbe changes sign on the negative part of the cycle, the directions of both ib and hfeib change together. Most texts do not explicitly show this, but it is worth bearing in mind that it would be perfectly valid to draw the small signal model as shown below with all directions reversed.

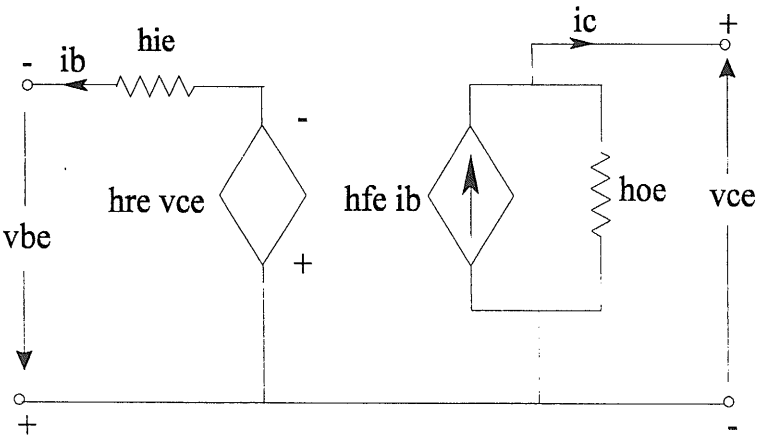

Figure 1.3 Alternative CE h parameter model with all signs reversed

Notice that in both Figures 1.2 and 1.3 the signs indicated a phase shift through the amplifier of 180° which is one of the main important practical applications of the small signal model in that it allows you to easily track phase through a circuit.
In analytical form Figures 1.2 and 1.3 may be represented by

$$vbe = hie\ ib + hre\ vce \tag{1.1}$$

$$ic = hfe\ ib + hoe\ vce \tag{1.2}$$

To determine hie, we set vce = 0 by shorting the collector to emitter through a low reactance and rearranging the remaining terms of the first equation giving

$$\text{hie} = \frac{\text{vbe}}{\text{ib}} \tag{1.3}$$

Note that vce = 0 does not imply that we can link the collector and emitter directly together to determine hie. We are dealing with small signal quantities and vce = 0 means that small changes are set to zero (an AC short). We are still left with the underlying DC voltage Vce which is the collector/emitter quiescent voltage. In the past it was common for authors to write the small signal model equations above in the form

$$\delta\text{Vbe} = \text{hie}\ \delta\text{Ib} + \text{hre}\ \delta\text{Vce} \tag{1.4}$$

$$\delta\text{Ic} = \text{hfe}\ \delta\text{Ib} + \text{hoe}\ \delta\text{Vce} \tag{1.5}$$

where Vbe, Ib, Vce and Ic are all DC quiescent quantities and the δ operator signifies "small change". Although this nomenclature is a little more clumsy than the present system it did help the reader avoid the common pitfall of misinterpreting the small signal model equations.

From (1.2) again with vce = 0 (low reactance between collector and emitter)

$$\text{hfe} = \frac{\text{ic}}{\text{ib}} \tag{1.6}$$

The remaining two parameters hre and hoe may be determined in a similar manner to hie except that the terms involving ib need to be removed from (1.1) and (1.2). Therefore setting ib = 0 (input open circuited)

$$\text{hre} = \frac{\text{vbe}}{\text{vce}} \tag{1.7}$$

and

$$\text{hoe} = \frac{\text{ic}}{\text{vbe}} \tag{1.8}$$

Measurement of hie, hfe

In practice determination of hie and hfe may be carried out by using the circuit below with C2 chosen to be as large as possible

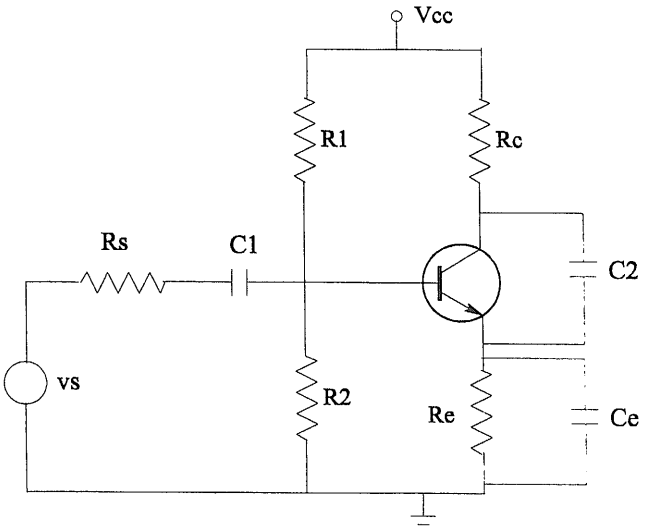

Figure 1.4 CE single stage amplifier configured for determination of hie and hfe

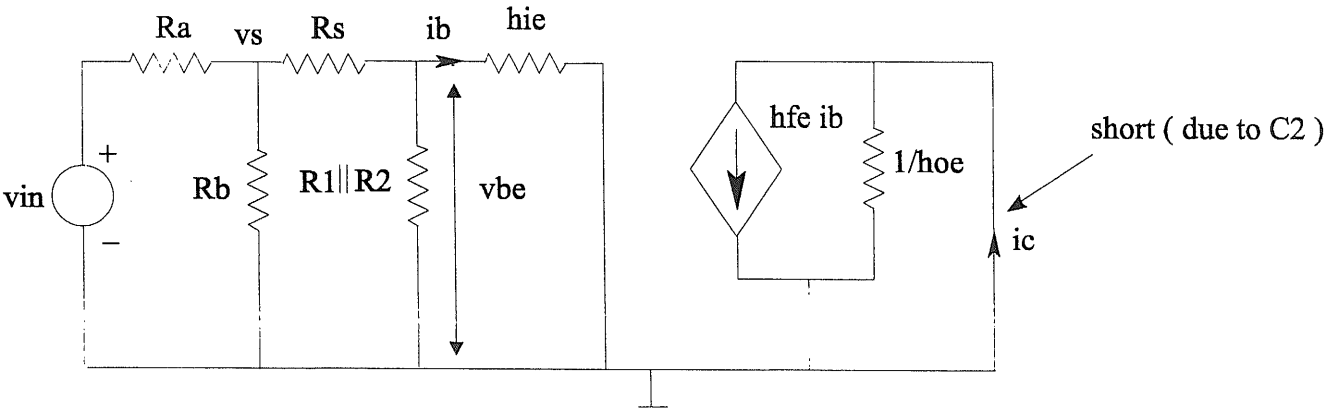

Figure 1.5 Small signal model corresponding to Figure 1.4

From Figure 1.5 the incremental base resistance hie is determined as

$$hie = \frac{vbe}{ib} \tag{1.9}$$

Either peak values or RMS values of vin and ib may be used to determine hie. The main consideration is that no DC component should be introduced into the ratio vbe/ib.

Direct measurement of ib may be unsatisfactory since it is usually small and subject to uncertainty introduced by noise.
Therefore as an alternative the following approach is suggested for the determination of hie.

If in Figure 1.5 Rp = R1|| R2 , vbe as a function of vs is given by

$$vbe = \frac{vs(Rp\ hie/(Rp + hie))}{Rs + Rp\ hie/(Rp + hie)} \tag{1.10}$$

Rearranging the above in terms of hie

$$hie = \frac{Rs}{\frac{vs}{vbe} - \frac{Rs}{Rp} - 1} \tag{1.11}$$

If Rs << Rp this would reduce to

$$hie = \frac{Rs}{\frac{vs}{vbe} - 1} \tag{1.12}$$

Note that by using the ratio vs/vbe as the measured variable an advantage is gained in that if the same instrument is used for both vbe and vs any bias or offset errors in the measurement may be effectively reduced.

In determining hfe via (1.6) you should encounter little difficulty in measuring ic. However as indicated above ib will be small and noise may severely corrupt the waveform. A suggestion here is that you should consider rearranging (1.6) and replace ib with a voltage and appropriate circuit resistances. Then measure the voltage and by analysis obtain ib.

An alternative approach (use as check) to the determination of hie is by way of the base/emitter junction IV characteristics shown below for a typical BJT. If the DC base current is the only current flowing through the base/emitter junction (Ic = 0), the reciprocal of the slope of the IV characteristics determines the value of hie. Note from the graph that because of the non-linear IV characteristic, shifts in the position of the quiescent point result in different values for hie. Particularly in the near neighborhood of the cut in point, hie can change considerably for small changes in the DC quiescent point and also may be significantly different from values quoted by the transistor manufacturer.

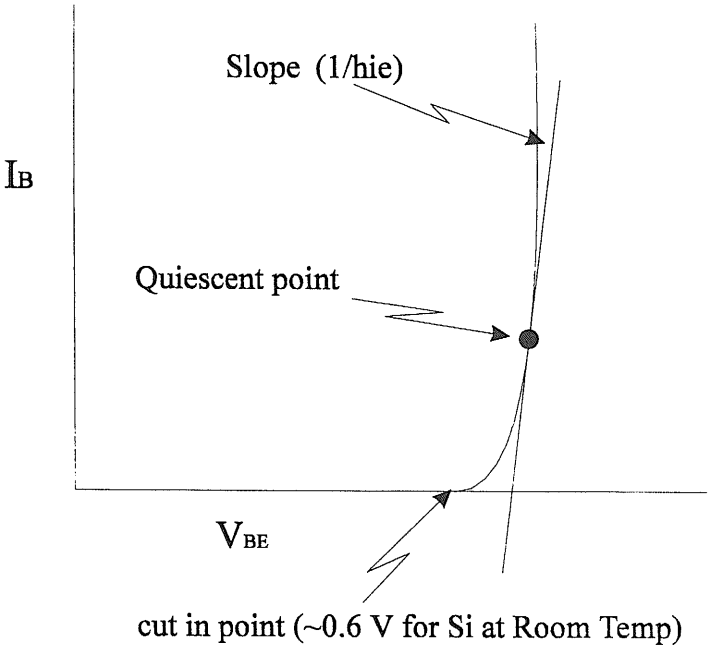

Figure 1.6 Typical BJT base/emitter characteristics

The base/emitter junction of each transistor may to a first order be modeled as an ideal diode. The ideal diode equation is written to remind you as

$$I_B = Io\exp(\frac{V_{BE}}{\eta V_T} - 1) \tag{1.13}$$

Note that in using this ideal diode equation for the BJT only the base current is considered as crossing the base/emitter junction here and Ic = 0.
The ideality factor η is usually taken as 1 for BJT's . We would also expect to be working beyond the cut in point where

$$\frac{V_{BE}}{\eta V_T} >> 1 \tag{1.14}$$

Rearranging (1.14)

$$V_{BE} = V_T \ln(\frac{I_B}{I_O}) \tag{1.15}$$

Differentiating (1.15) yields a value for hie

$$\frac{\partial V_{BE}}{\partial I_B} = hie = \frac{V_T}{I_B} \tag{1.16}$$

Note that this is an ideal value and does not include contributions to hie from the base spreading resistance or the emitter region resistance.

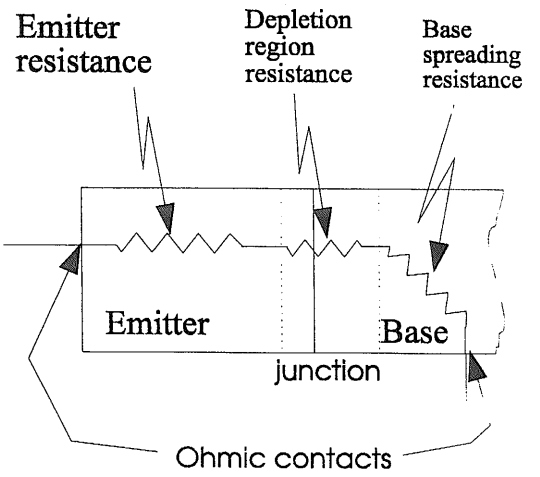

Figure 1.7 Components of base/emitter resistance included in hie

In practice there are four component parts to hie as shown above

(1) Ohmic contacts at base and emitter
(2) the emitter resistance
(3) depletion region resistance
(4) base spreading resistance

The "ohmic" contact between the emitter and the outside wiring is so called because the manufacturer attempts to make this interface linear (i.e. obey Ohm's law - unlike the base emitter junction V I characteristic). At the same time this resistance is minimized so that unwanted power dissipation is reduced. A similar design strategy is adopted with the interface between the base and the outside world. The result is that these two interfaces contribute only a small part of the total base/emitter resistance.

Usually the emitter region is relatively highly doped so that the contribution from (2) is small compared with (3) and (4). The base/emitter junction is always forward biased in the normal amplifier mode so that the depletion region is relatively narrow and its resistance is perhaps 10% to 20% of the total depending on the transistor type. The base region is usually lightly doped and forms a significant part of hie via the base spreading resistance. The reason that this base resistance is often referred to as the base spreading resistance is that one end of the equivalent resistor is the base terminal while the other end consists not of a readily identifiable point but the base emitter junction cross sectional area.

Measurement of hoe, hre

Using equations (1.7) and (1.8) the circuit shown in Figure 1.8 allows determination of hoe and hre. It should be remembered that these values are somewhat extreme and that the uncertainties involved in the measurement will be a limiting issue.

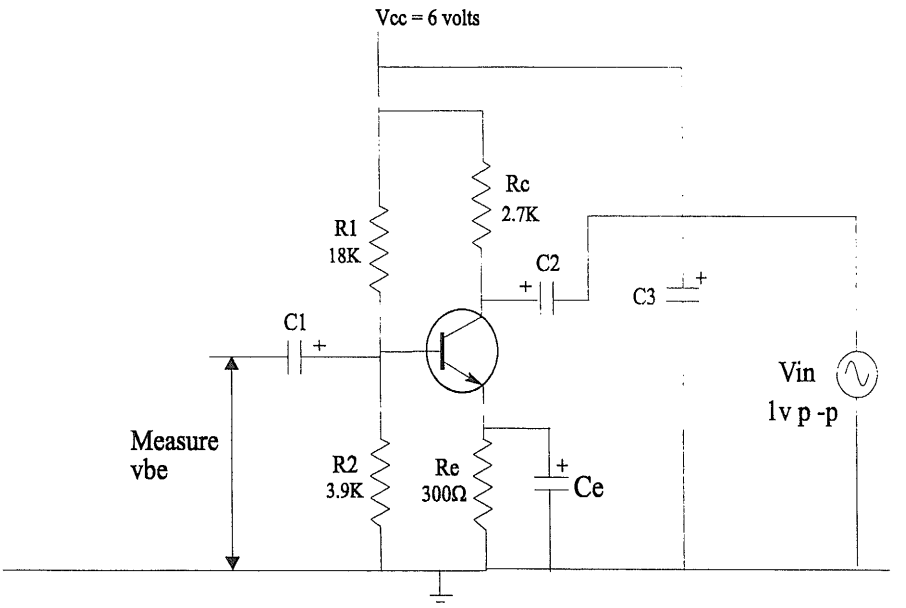

Figure 1.8. Modification for the measurement of hre and hoe

EE LABORATORY IV

ECE 312

Experiment 2. Operational Amplifiers

PURPOSE:

This lab introduces the operational Amplifier (OP-Amp) as an active circuit element in electronic systems and examines different configurations. You are required to design and implement several circuits which illustrate practical uses of this device.

EQUIPMENT REQUIRED:

1 OP-Amp μ741
1 CEU Electronic system development station
Resistors as noted

INTRODUCTION:

The OP-Amp is an integrated differential voltage amplifier. It is used in many fields of technology as a summer, wide band amplifier, comparator and signal processing element in communications and control. The device is so-named because it is used to carry out "operations" on signals . The symbolic representation is: -

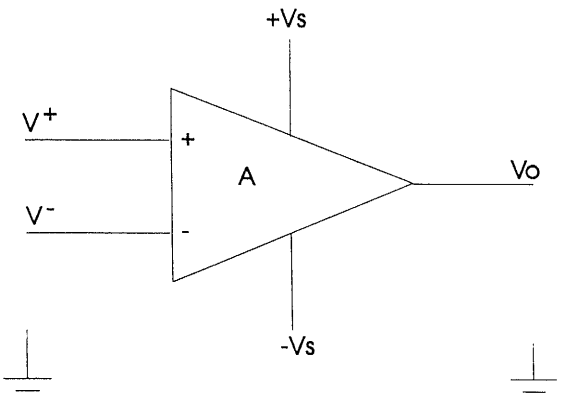

Figure 2.1 Basic operational amplifier configuration

Note that often in texts and in most cases throughout this sequence of experiments the power supply connections ±Vs are not shown explicitly. If you do not connect the power supplies no damage will be done. However your circuit also will not work (at all !).
The equation linking the input and output for this device is :-

$$v_0 = A(v^+ - v^-) \tag{2.1}$$

The input labelled "+" indicates non-inverting operation between input and output. The input labelled "-" indicates inverting operation or 180° phase shift between input and output (for an ideal amplifier or a "real" amplifier at low frequencies). For most applications the Op-Amp may be considered **ideal.** A simple equivalent circuit available in PSPICE which represents a simple **non-ideal** amplifier is the following.

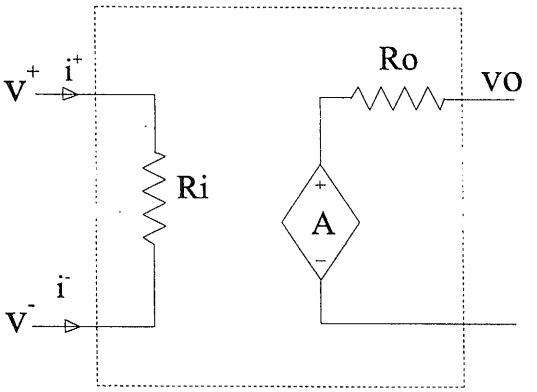

Figure 2.2 Simple non-ideal model for the OPAMP

In comparing ideal and non ideal devices the following characteristics may be listed :-

	Ideal Op Amp	**μA741**
1.	Input impedance Ri = ∞	Ri = 2 M
2.	Output impedance Ro = 0	Ro = 75 Ω
3.	Voltage gain A = ∞	A = 20,000 – 200,000
4.	Bandwidth = ∞	Unity Gain BW- 1 MHz
5.	Vo = 0 if $V^+ = V^-$	CMRR – 90 dB

For most applications it is adequate to treat the amplifier in your circuit as ideal. With infinite impedance apparent at each input terminal for **the ideal case, no current can flow into either input.** This means that output current is derived from the ±Vs DC power supply and no power is extracted from the input signal even if the amplifier is processing an a.c. waveform. The gain of an operational amplifier is high (note the figure above for the μA741) but the output voltage cannot exceed the DC power supply level. This means that the voltage between the inputs must be relatively small. **In the ideal case this differential input voltage is considered to be zero**

so that analysis proceeds on the basis that $v^+ = v^-$. For example: If the power supplies Vs = ±10 volts, the ideal maximum peak to peak value of the output signal that can be obtained from the amplifier without distortion is 20 volts. Any attempt to produce a larger signal will result in the amplifier being driven into saturation (non-linear operation) and clipping will occur. The input signal $(v^+ - v^-)$ required to produce this output using the μA741 in the open loop mode using equation (2.1) is ≤ 1mV (not zero but small !.)

PROCEDURE

Part 1 - Inverting Amplifier

By drawing on the results of the theory section, design a closed loop operational amplifier system which meets the following specification at low frequencies

Input Resistance = 1 kilohm
Closed loop gain = -20
Power supplies = ±10 volts

Before testing the circuit in hardware form, simulate the circuit using PSPICE and confirm both the system gain and input resistance. Use a DC source for your simulation.

Only when you have completed the design and simulation and obtained satisfactory results should you wire up and test the circuit in hardware form. Use the preferred resistance values nearest to the theoretical values you obtained. Test the system and confirm gain and input resistance for a sine wave input of 1 kHz and appropriate amplitude.

Part 2 - Non-inverting Amplifier

Using the theory section again, design a closed loop operational amplifier which meets the following specification at low frequencies

Input Resistance = 33 kilohms
Closed loop gain = + 11
Power Supplies = ± 10 Volts

As in part 1, only when you have completed the design and simulation and obtained satisfactory results should you wire up and test the circuit in hardware form. Use the preferred resistance values nearest to the theoretical values you obtained from theory. The test waveform should be 1 kHz with appropriate amplitude.

Part 4. Negative Impedance Converter

Using the circuit shown below determine appropriate circuit impedance (resistance or reactance) values to meet the following specification at low or intermediate frequencies :-

Zin = -10k (negative)

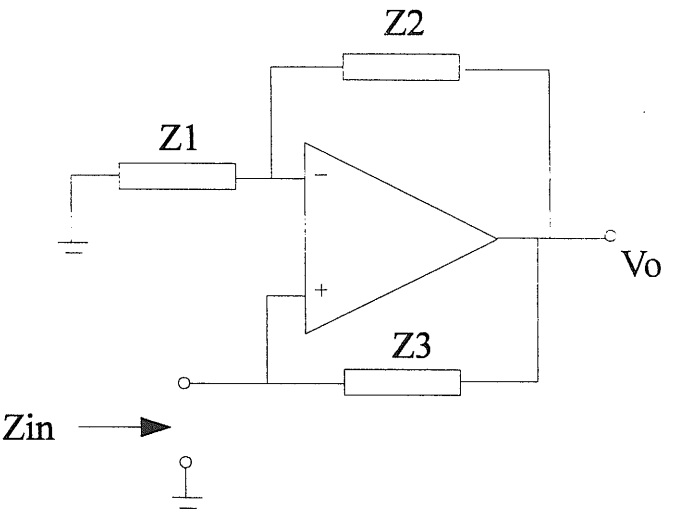

Figure 2.3 Negative Impedance Converter

As in previous sections when you have completed the design to your satisfaction simulate it and then implement the circuit in hardware. Establish by measurement that the circuit meets your design goal.

OPERATIONAL AMPLIFIER - THEORY

The following section is based on the assumption that the amplifier is **ideal** as indicated in the introduction. In terms of the following analyses this means that there is negligible voltage difference between two inputs and no current may flow into either input. These two assumptions are fundamental to developing input/output relationships for OPAMP systems.

Inverting Amplifier - Input/output relationship

The currents and voltages vin and i1, i2 are either DC or instantaneous values

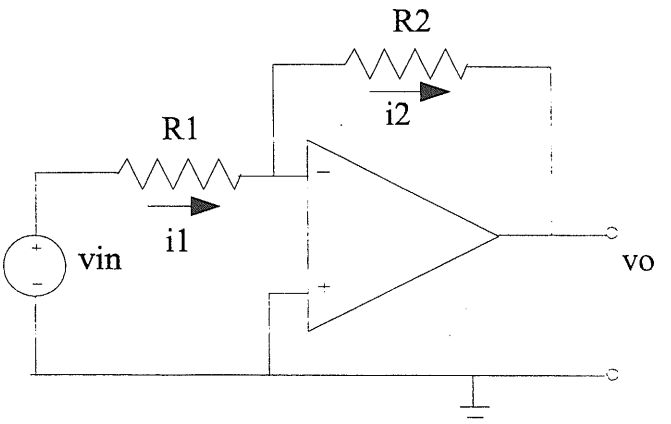

Figure 2.4 Inverting Amplifier Configuration

Since no current flows into either input

$$i1 = 12 \tag{2.2}$$

The voltage between inputs is considered to be zero and with the non-inverting input connected directly to ground, the voltage at the inverting input is also zero with respect to ground. Therefore (2.2) may be written in terms of voltage as :-

$$\frac{(vin - 0)}{R1} = \frac{(0 - vo)}{R2} \tag{2.3}$$

Rearranging (2.3) gives :-

$$\frac{vo}{vi} = -\frac{R2}{R1} \tag{2.4}$$

The overall gain depends only on the ratio of the two resistors in the circuit. The negative sign implies phase inversion between the input and output. Feedback has suppressed the effect of the open loop gain A which was taken to be high (ideally infinite).

Inverting Amplifier - Input resistance

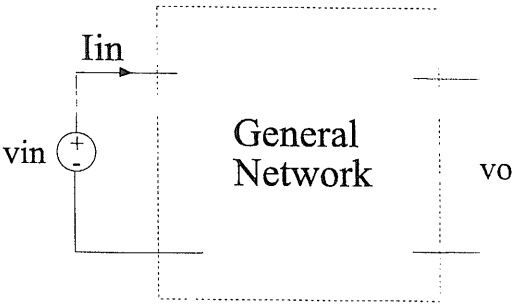

Figure 2.5 Input impedance of general linear network

For any **linear** system the input impedance is given by the following ratio

$$Zin = \frac{vin}{iin} \tag{2.5}$$

Therefore in general the input impedance of a circuit may be found by connecting a test voltage source to the network of interest and measuring the current driven into the circuit by that test voltage source. If the impedance has a reactive component the frequency and the amplitude of the input test signal must obviously be considered. In the case of a circuit that involves active devices it is essential that the test voltage source not interfere with the normal DC bias of the circuit. In this case the test voltage source should be coupled to the circuit of interest through a capacitance of very low reactance at the frequencies of interest.

For the operational amplifier it has already been stated that if the amplifer is ideal no current may flow into either input. In applying (2.5) to this case one might expect at first thought that the input resistance should be infinity since no current flows into the amplifier input. However the whole circuit including feedback must be accounted for. Redrawing the first order non-ideal circuit shown in Figure 2.2 and including the input and feedback resistors which forms the full inverting amplifier the following circuit emerges

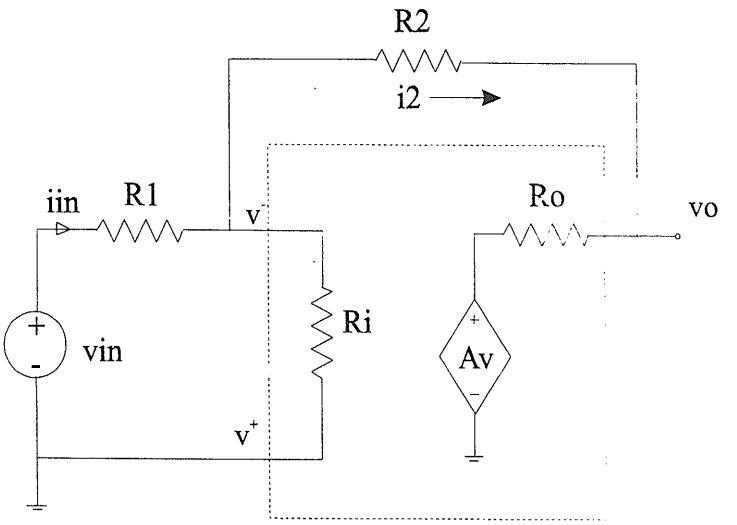

Figure 2.6 Inverting amplifier including first order non-ideal model

It would not be too difficult to analyze the complete circuit including the non-ideal components Ri, Av and Ro to obtain the input impedance. However since in ECE 321 we are concerned primarily with a treatment of the ideal amplifier a simpler approach is adopted. Writing the loop equation round the loop including vin, R1, R2 and the output

$$vin = iinR1 + i2R2 + vo \tag{2.6}$$

The input /output relationship for the ideal case has already been shown to be

$$\frac{vo}{vin} = \frac{-R2}{R1} \tag{2.7}$$

so that substituting in (2.6)

$$vin = iinR1 + (i2R2 - \frac{R2}{R1} vin) \tag{2.8}$$

However if the voltage between the inverting and non-inverting inputs is negligible

$$i2R2 = (0 - vo) \tag{2.9}$$

Substituting from (2.9) into (2.8) the terms in parentheses are shown to sum to zero and we are left with

$$\frac{vin}{iin} = R1 \tag{2.10}$$

Non-inverting Amplifier - Input/output Relationship

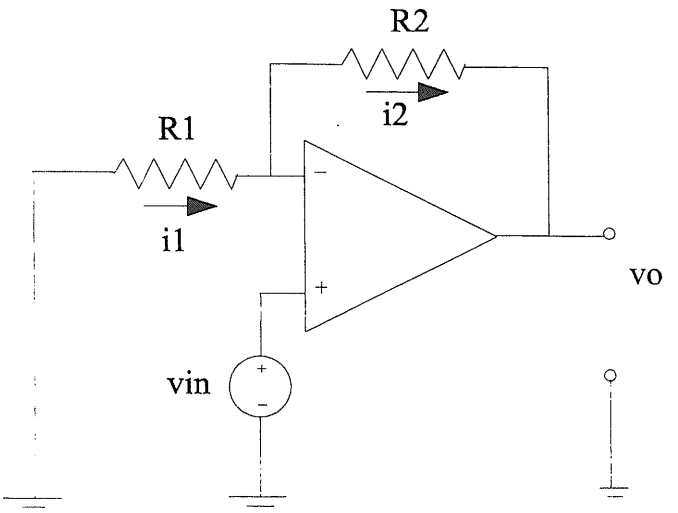

Figure 2.7 The non-inverting Amplifier

Analysis begins in the same way as for the inverting amplifier. Since no current flows into either input :-

$$i1 = i2 \tag{2.11}$$

In this case the voltage at each input is vin so that in manipulating equation (2.11) into voltage terms the following result is obtained :-

$$\frac{(0 - \text{vin})}{\text{R1}} = \frac{(\text{vin} - \text{vo})}{\text{R2}} \tag{2.12}$$

Rearranging equation (2.12) yields

$$\frac{\text{vo}}{\text{vin}} = \frac{\text{R1} + \text{R2}}{\text{R1}} \tag{2.13}$$

This result shows no phase inversion and again the overall gain depends only on the resistances.

Non-inverting Amplifier - Input Resistance

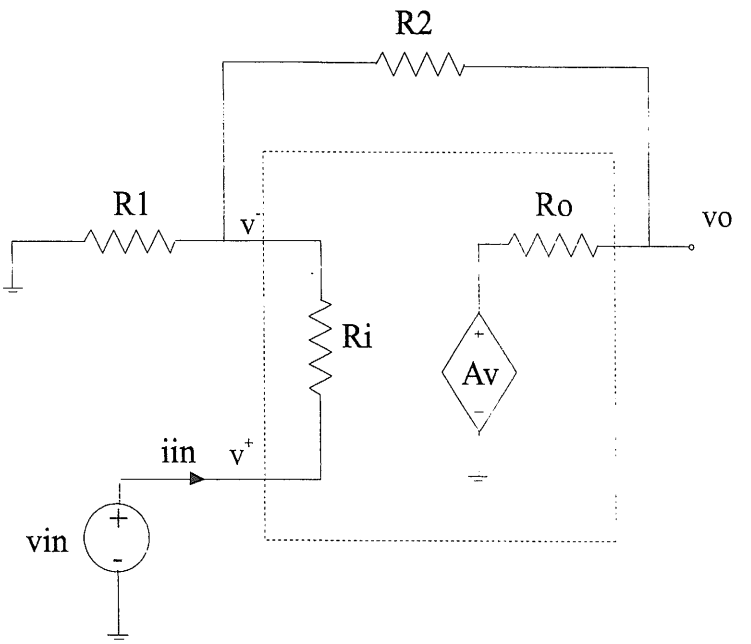

Figure 2.8 The non-inverting amplifer including first order non-ideal model

For the circuit of Figure 2.8 taking the ratio of the test voltage vin versus iin in the general case would not be very difficult. However for the ideal case it is simple since Ri is considered infinity. Therefore iin = 0 (ie no current flows into either input) and

$$Zin = \frac{vin}{iin} = \infty \tag{2.14}$$

The Integrating Amplifier

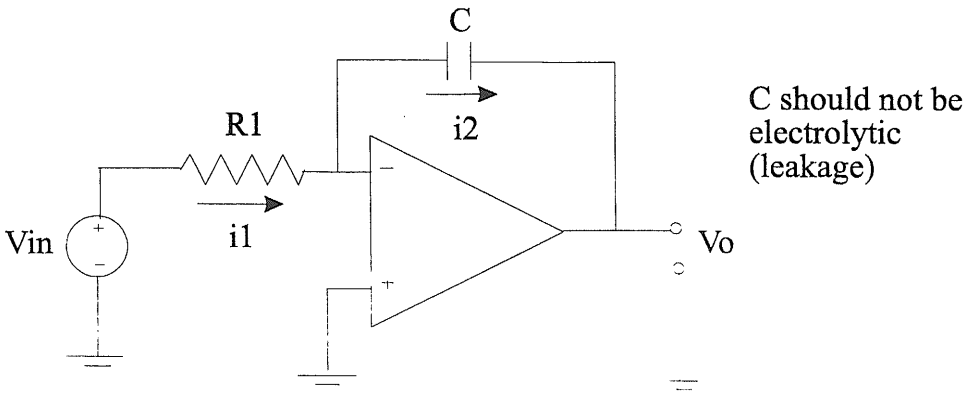

Figure 2.9 The integrating Amplifier

Figure 2.9 shows the inverting integrator which is of the same form as the inverting amplifier except that the feedback resistance is replaced with a capacitance C1. Analysis proceeds in exactly the same manner as the two previous amplifers. No current flows into either amplifier input so that

$$i1 = i2 \tag{2.15}$$

The voltage between inputs is considered to be zero and with the non-inverting input connected directly to ground just as with the inverting amplifier, the voltage at the inverting input is also zero with respect to ground. Therefore taking into account the current diection i2 may be written

$$i2 = C1\frac{d(0 - vo)}{dt}$$

or

$$i2 = -C1\frac{dvo}{dt} \tag{2.16}$$

Therefore (2.15) may be written in terms of voltage as :-

$$\frac{(\text{vin} - 0)}{\text{R1}} = -\text{C1}\frac{\text{dvo}}{\text{dt}} \tag{2.17}$$

Rearranging (2.17) gives :-

$$vo = -\frac{1}{R1.C1}\int vin.dt \tag{2.18}$$

The Negative Impedance Converter

This circuit forms the basis of several useful applications. It can be used as a current source and in forming positive impedance cancelling elements. The basic circuit is as shown below

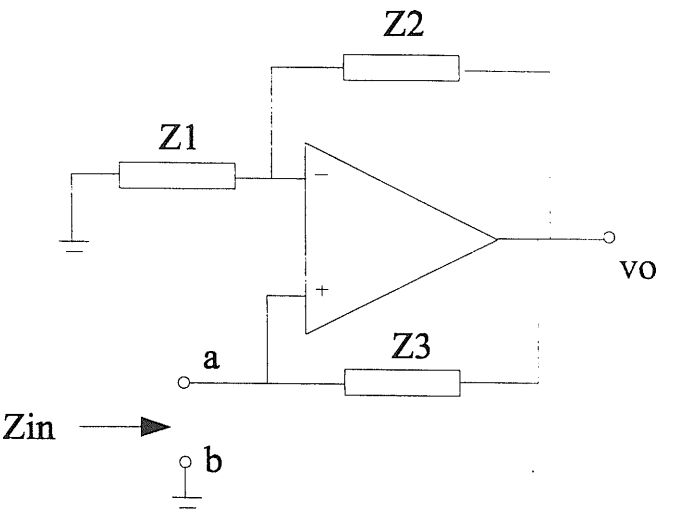

Figure 2.10 The Negative Impedance Converter

The circuit input impedance is given by

$$Zin = \frac{vin}{iin} \tag{2.19}$$

Due to the ideal amplifier assumption

$$v^+ = v^- = vin \tag{2.20}$$

where Vin is a test voltage injected between the points a and b shown in Figure 2.10 and iin is the current driven into the circuit by this voltage.

The inverting and non-inverting input voltages are given by

$$v^+ = v^- = vo\frac{Z1}{Z1+Z2} \tag{2.21}$$

This equation is valid provided the differential input impedance between the inverting and non-inverting inputs is very large as should be the case for all practical amplifiers. In the ideal case it is of course infinity.
Since no current flows into the non-inverting input for the ideal case

$$\text{iin} = \frac{\text{vin} - \text{vo}}{\text{Z3}} \tag{2.22}$$

or

$$\text{vin} = \text{Z3 iin} + \text{vo} \tag{2.23}$$

However from (2.21)

$$\text{vo} = \frac{\text{v}^{+}(\text{Z1} + \text{Z2})}{\text{Z1}} \tag{2.24}$$

Substituting from (2.24) into (2.23) for vo

$$\text{vin} = \text{iin Z3} + \frac{\text{vin}(\text{Z1} + \text{Z2})}{\text{Z1}} \tag{2.25}$$

or

$$vin\left[1 - \frac{(\text{Z1} + \text{Z2})}{\text{Z1}}\right] = iin\,Z3 \tag{2.26}$$

Writing (2.26) in terms of input resistance

$$\text{Zin} = \frac{\text{vin}}{\text{iin}} = \frac{\text{Z3}}{1 - \frac{(\text{Z1} + \text{Z2})}{\text{Z1}}} \tag{2.27}$$

Rearranging (2.27) gives

$$\text{Zin} = -\frac{\text{Z1 Z3}}{\text{Z2}} \tag{2.28}$$

Note that this impedance is negative. An obvious first check of this equation is to allow Z3 to go to infinity. We should expect that the input impedance should also tend to infinity since the configuration becomes a non-inverting amplifier.

EE LABORATORY IV

ECE 312

Experiment 3. Active Current Sources

PURPOSE:

This laboratory provides experience in the analysis and design of active current sources and their application in linear integrated circuits.

EQUIPMENT NEEDED:

1 Transistor Array CA3046
1 CEU Electronic System Development Station
Resistors as required

INTRODUCTION

Apart form the obvious need for active devices to provide amplifying capability in linear integrated circuits there are three other principal uses for active devices in linear integrated circuits. These are

(1) Current Sources
(2) Active Loads
(3) Level Shift

Current sources may be used in several applications in a linear integrated circuit. It is shown in the theory section of the differential amplifier laboratory that it is an advantage for the behavior of a differential amplifier if the emitter resistance is as large as possible. However in integrated circuit technology it is undesirable to fabricate large resistors because of the space they consume, so an independent current source is frequently used instead.

As a reminder the terminal characteristics of a current source are shown in Figure 3.1(a) together with the circuit model in Figure 3.1(b). The resistance ro should be large otherwise current will vary significantly with voltage. In the case of the ideal current source $ro = \infty$ and the slope of the IV characteristic shown is zero. In general a major goal in designing current sources is to try to reproduce the characteristics of the model shown in Figure 3.1(b) using active devices with ro as high as possible.

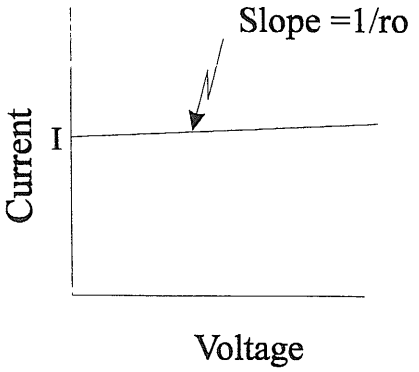

Figure 3.1(a) Current Source Characteristics

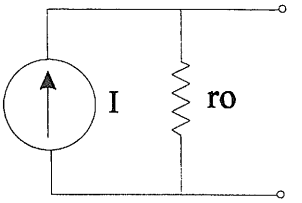

Figure 3.1(b) Current Source Model

PROCEDURE

Part 1 - Design an active current source using two transistors of the CA3046 Array which meets the specification given in graphical form in Figure 3.2 to better than ±5%. The circuit you should use is given in Figure 3.3. The power supply should be 10 Volts and your design should be complete before you try implementing it in hardware. Note that you are not attempting to design the "best" current source but you should be aiming at just meeting the specifications.

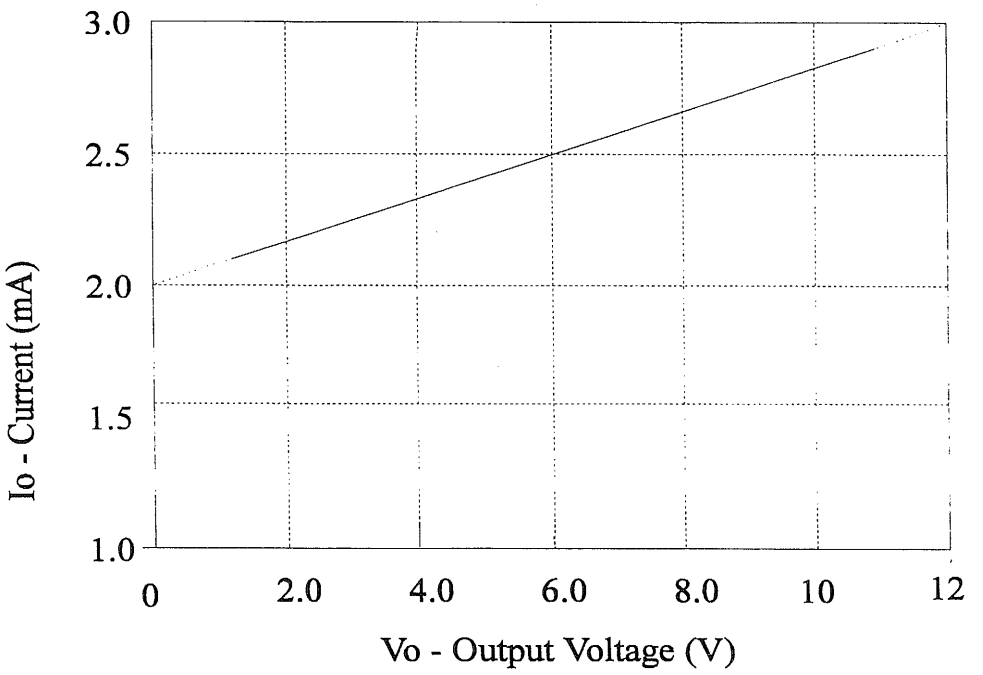

Figure 3.2 The required load behavior of Simple Current Source Design

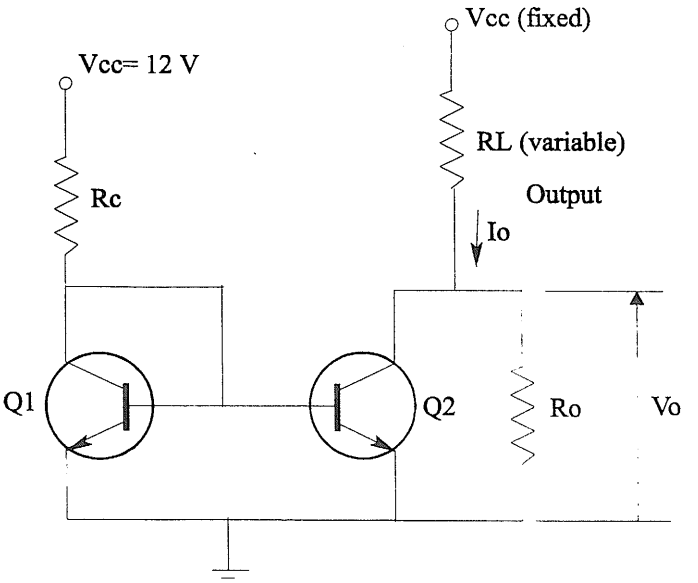

Figure 3.3 Simple Current Source - Circuit to be used in Part 1

Part 2. Design a Widlar current source which will give a current output of 100 μA with an output resistance of greater than 200 K. Over the output voltage range 3 - 7 volts thecurrent should meet the specification Io = 100 ± 20μA. Use the CA3046 Array as in Part 1

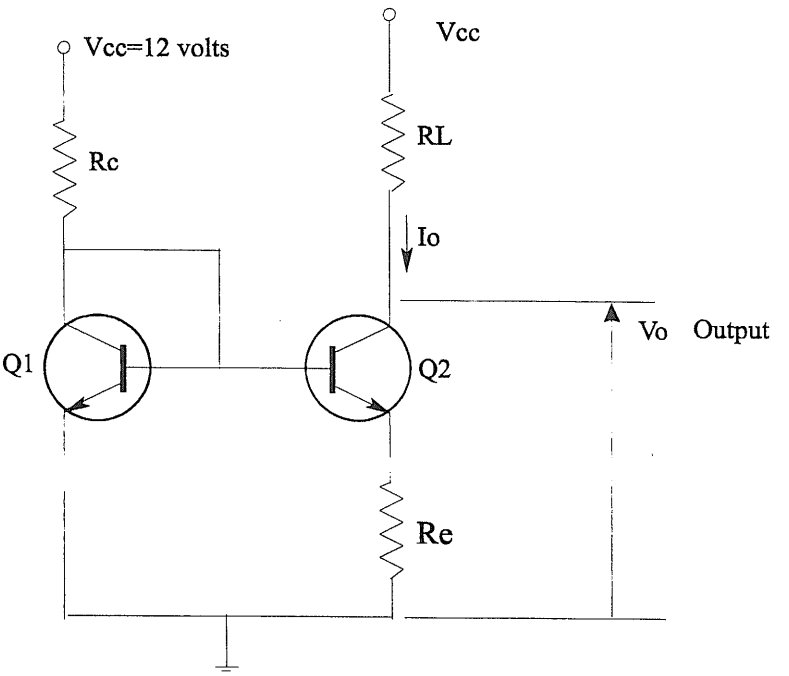

Figure 3.4 Widlar Source to be used in Part 2

ACTIVE CURRENT SOURCES - THEORY

A simple current source may be implemented by using the following circuit

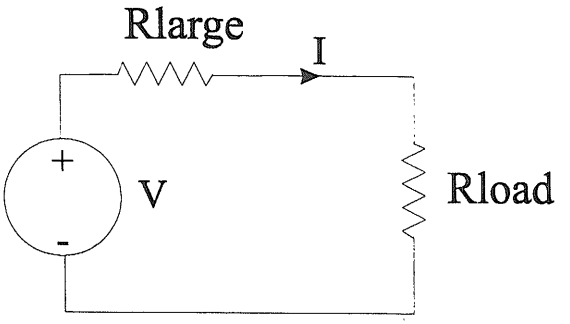

Figure 3.5 Simple Current Source

The current for a simple source is given by

$$I = \frac{V}{Rs + Rload} \tag{3.1}$$

If Rload <<Rs variations in the load will not significantly affect the magnitude of current supplied by the voltage source which will be given by

$$I \cong \frac{V}{Rs} \tag{3.2}$$

Unfortunately in integrated circuit technology it is undesirable to implement large resistors directly from a space point of view, so the simple current source is not particularly useful depending as it does upon the use of a large resistance. In addition significant current generation would require a high voltqge source which also is not practical for integrated circuit use.

The Simple Active Current Source

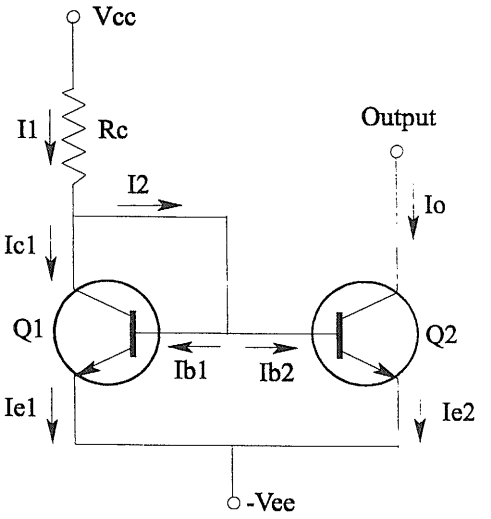

Figure 3.6 The Simple Active Current Source

The DC behavior of the circuit shown in Figure 3.6 is examined by noting that the transistors Q1 and Q2 may be considered identical since they are fabricated on the same chip. The large signal currrent gain β (h_{FE}) will be the same for both transistors and since the base/ emitter junctions are also considered identical the current I2 divides equally between the bases giving

$$Ib1 = Ib2 \tag{3.3}$$

and

$$I2 = 2Ib1 \tag{3.4}$$

Using KCL at the collector of Q1

$$I1 = Ic1 + I2 \tag{3.5}$$

and

$$Ie1 = Ib1 + Ic1 = Ib1(1+\beta)$$

or

$$Ib1 = \frac{Ie1}{(1+\beta)} \tag{3.6}$$

The collector currents for either transistor may now be written as

$$Ic1 = Io = \frac{\beta.Ie1}{(1+\beta)} = \frac{\beta.Ie2}{(1+\beta)} \tag{3.7}$$

Notice that Io does not appear to depend on the collector load of Q2. This is a fundamental requirement for a current source .
The relationship between I1 and Io may be deduced by rearranging (3.5)

$$I1 = Ic1 + I2$$

or

$$I1 = \frac{\beta(Ie1)}{(1+\beta)} + \frac{2(Ie1)}{(1+\beta)} = \frac{(2+\beta)Ie1}{(1+\beta)} \tag{3.8}$$

From (3.5) and (3.7)

$$\frac{Io}{I1} = \frac{\beta(Ie2)/(1+\beta)}{(2+\beta)Ie2/(1+\beta)} = \frac{\beta}{2+\beta} = \frac{1}{1+2/\beta} \cong 1 \tag{3.9}$$

Output resistance of simple current source

In using the hybrid parameters as a tool to deduce the output resistance of a current source a danger exists that we might be tempted to claim more than is possible. All hybrid parameters vary with changes in the active device quiescent operating point. It is stressed as in previous theory sections that these hybrid parameters are small signal parameters. We are proposing (as do many texts) to use them in what is essentially large signal conditions - the variation of output current for different load conditions. With this in mind the small signal model using hybrid parameters for the simple active source is shown in Figure 3.7. Since the emitter of transistor Q2 is returned directly to ground the output resistance is given by

$$\text{Rout} = \frac{1}{\text{hoe}} = \text{ro} \tag{3.10}$$

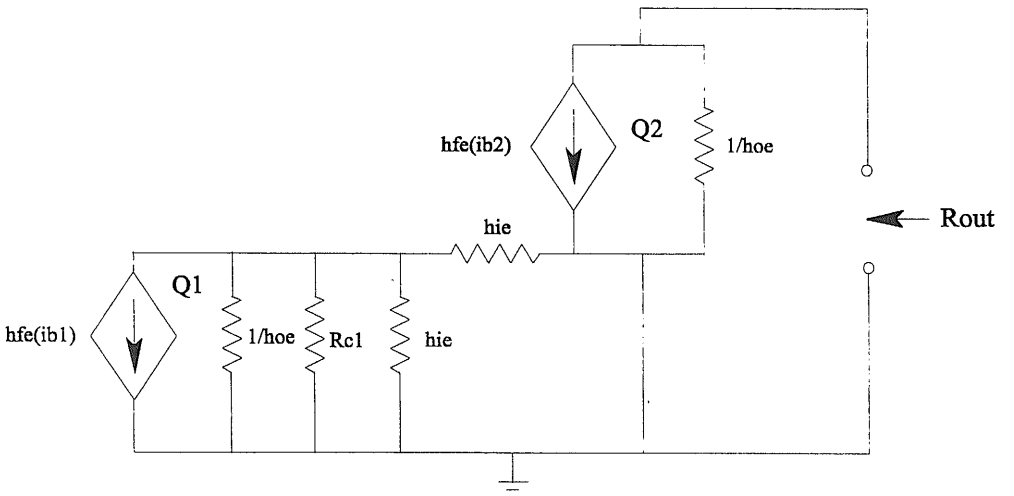

Figure 3.7 Model of Simple Active Source

The Widlar Current Source

The tranisistor output collector resistance of the simple current source ro or 1/hoe is usually several kilohms but this may not be high enough to result in a satisfactory current source for integrated circuits. One way to improve the situation is to replace the emitter to ground short circuit of transistor Q2 by a large emitter resistance . This leads to the following which has been named after R. S. Widlar who first proposed the circuit in 1968

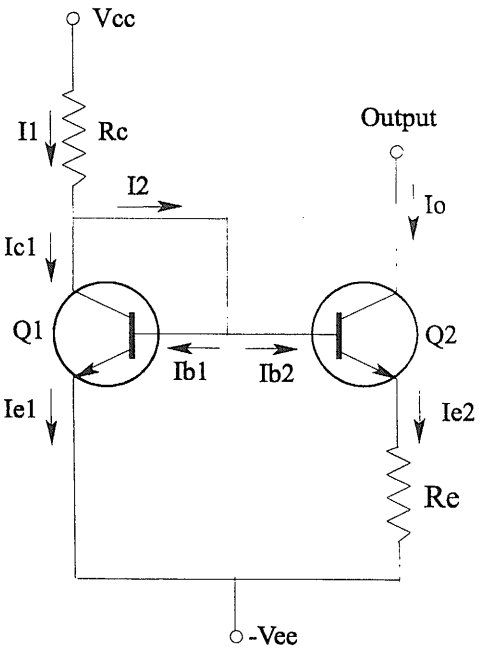

Figure 3.8 The Widlar current source

In comparison with the simple current source it is evident that total symmetry between both sides of the circuit has been lost and we can no longer assume that the base currents are identical. To determine the output current the loop equation including each of the base/emitter junctions is written as

$$V_{BE1} - V_{BE2} = I_{E2} R_e \tag{3.11}$$

The base/emitter junction of each transistor may be modelled as an ideal diode. The ideal diode equation is written to remind you as

$$I_E = I_s \exp\left(\frac{V_{BE}}{\eta V_T} - 1\right) \tag{3.12}$$

The ideality factor η is usually taken as 1 for BJT's . We would also expect to be working well beyond the cut in point where

$$\frac{V_{BE}}{\eta V_T} >> 1 \tag{3.13}$$

(3.12) may therefore be rearranged as

$$V_{BE} = V_T \ln(\frac{I_E}{Is}) \tag{3.14}$$

Substituting this in (3.11)

$$V_T \ln(\frac{I_{E1}}{Is}) - V_T \ln(\frac{I_{E2}}{Is}) = I_{E2} R_E \tag{3.15}$$

Rearranging

$$V_T \ln(\frac{I_{E1}}{I_{E2}}) = I_{E2} R_E \tag{3.16}$$

Q1 and Q2 are assumed matched so that V_T and α are the same for both. Therefore multiplying (3.16) through by α enables the relationship between the collector currents to be writtten as

$$IoR_E = V_T \ln(\frac{I_{C1}}{Io}) \tag{3.17}$$

Output Resistance of Widlar current source

The small signal model is given in Figure 3.9.

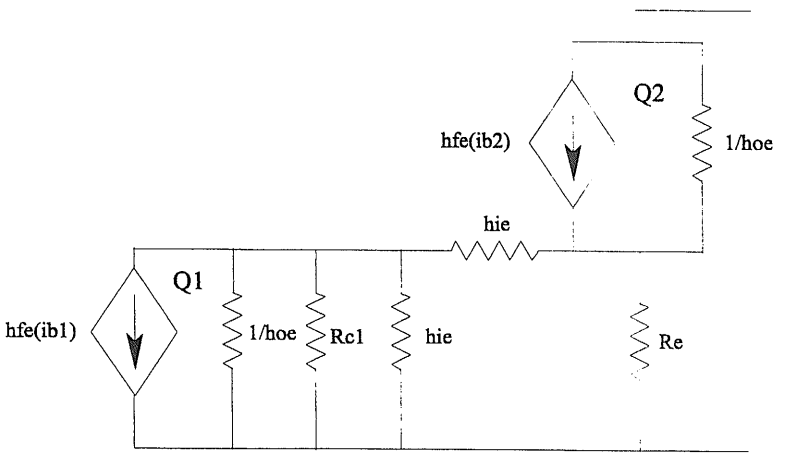

Figure 3.9 The small signal model for the Widlar Current Source

At first glance it would appear that obtaining the output resistance is a relatively complicated operation. However note that the base/collector junction of transistor Q1 is shown short circuited. This is significant in that the transistor output conductance hoe is largely determined by this junction which is reverse biased in the normal amplifying mode of operation. This results is a relatively low value for 1/hoe for Q1 which may be modelled as short circuit.

In order to determine the output resistance a test voltage vth is intoduced and the circuit of Figure 3.10 results

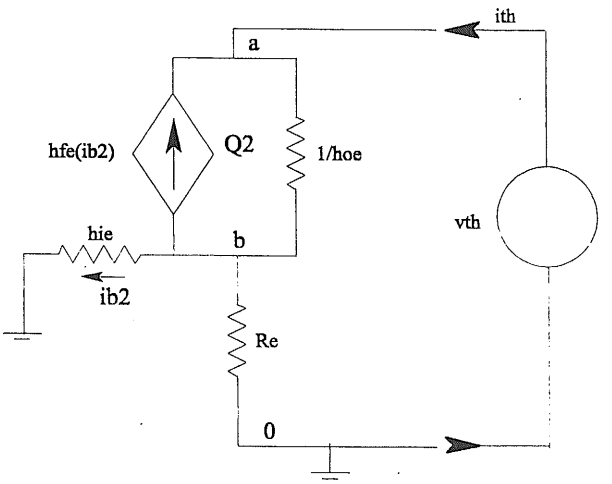

Figure 3.10. Widlar Source Equivalent Small Signal Circuit

Understanding the rationale behind the directions of instantaneous currents in Figure 3.10 is particularly important. The only independent source in the circuit is the test voltage source vth which is shown driving instantaneous current ith into the node labelled a. The current return is via hie and Re in parallel. The instantaneous current ib2 through hie must therefore be in the direction shown by the arrow. The current supplied by the dependent current source is controlled in magnitude and direction by ib2. The direction of the current supplied by the dependent source hfe(ib2) should therefore be reversed when compared with the previous model (Figure 3.9). If you are concerned that this implies current passing out of the base terminal of an NPN transistor remember yet again that we are working in terms of instantaneous or small signal values. To find the output resistance Rout we need to find the ratio

$$\text{Rout} = \frac{\text{Vth}}{\text{ith}} \tag{3.18}$$

The thevenin test voltage is given by the summing the voltage drops across the circuit resistances

$$\text{vth} = \text{Vab} + \text{Vbo} \tag{3.19}$$

The voltage between nodes a and b is

$$\text{Vab} = (\text{ith} + \text{hfe.ib2})\frac{1}{\text{hoe}} \tag{3.20}$$

Similarly the voltage between node b and ground is given by

$$vbo = hie.ib2 \tag{3.21}$$

Substituting (3.20) and (3.21) into (3.19)

$$vth = (ith + hfe.ib2)\frac{1}{hoe} + hie.ib2 \tag{3.22}$$

We now need to write ib2 in the above equation in terms of ith so that when we divide through by ith Rout will emerge. Alternatively since the analysis is slightly simpler we will substitute for ith in terms of ib2 and make sure that when we divide to get Rout we will have ith also in terms of ib2 in the denominator. Writing KCL at node b gives

$$hfe.ib2 + ib2 + \frac{vbo}{Re} = vab.hoe \tag{3.23}$$

Substituting from (3.20) and (3.21) for vab and vbo yields

$$hfe.ib2 + ib2 + \frac{ib2.hie}{Re} = (ith + hfe.ib2)$$

or

$$ith = ib2(1 + \frac{hie}{Re}) \tag{3.24}$$

Substituting back into (3.22) for ith

$$vth = ib2(1 + \frac{hie}{Re} + hfe)1/hoe + hie.ib2 \tag{3.25}$$

Dividing through by ith

$$Rout = \frac{vth}{ith} = \frac{(1 + hie/Re + hfe)1/hoe + hie}{1 + hie/Re} \tag{3.26}$$

(3.26) is a general result and no assumptions are drawn concerning the relative magnitudes of parameters. Many texts make assumptions at this stage which are often completely unjustified for a particular practical case.

It was shown in Experiment 1 that

$$\text{hie} = \frac{\text{hfe}V_T}{\text{Ic2}} \tag{3.27}$$

where Ic2 is the output current in this case. Substituting for hie form (3.27) into (3.26)

$$\text{Rout} = \frac{(1 + \text{hfe}V_T/\text{Ic2}\,\text{Re} + \text{hfe})1/\text{hoe} + \text{hfe}V_T/\text{Ic2}\,\text{Re}}{1 + \text{hfe}V_T/\text{Ic2}\,\text{Re}} \tag{3.28}$$

EE LABORATORY IV

ECE 312

Experiment 4. BJT Differential Amplifiers

PURPOSE :

This laboratory provides an introduction to the analysis and design of integrated differential amplifiers.

EQUIPMENT REQUIRED :

1 Transistor Array CA3046
1 CEU Electronic System development station
Resistors as required

INTRODUCTION

It is likely that your previous experience with transistor amplifiers has been largely restricted to the use of discrete transistors. You will recall that associated with the design of both BJT and FET amplifiers is the need to maintain operation of the amplifier around a suitably chosen DC quiescent point. The designer must satisfy production needs when two transistors of the same type number have β's that could be as much as a factor of 5-10 different. Also the amplifier may be required to operate in an environment whose temperature may change. Both of these requirements are usually satisfied through the use of properly designed biasing networks.

Another approach to stabilization is to use transistors which are intended for operation in a differential mode. These are devices which are physically and electrically matched and built on the same substrate. Changes due to temperature swings affect both transistors of the matched pair similarly. Providing the transistors are used in a differential mode, the effects of temperature on the overall amplifier behavior are considerably reduced in comparison with a single transistor device. This approach is fundamental to the design of modern integrated operational amplifiers.

PROCEDURE

Part 1 - Amplifier Design

The circuit for a simple differential amplifier or "long tailed pair" is shown in Figure 4.1.

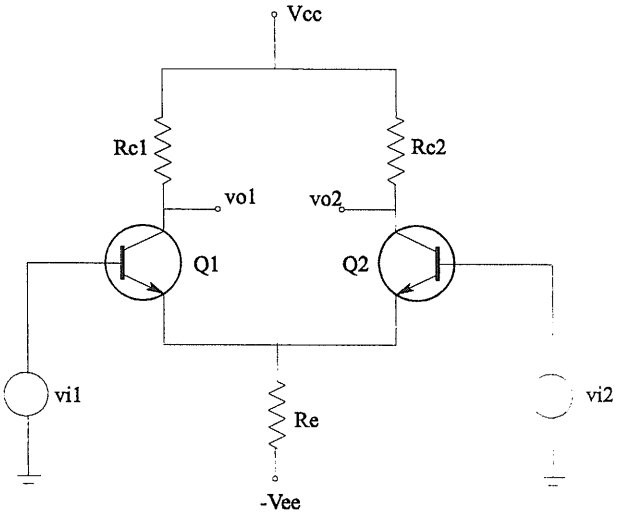

Figure 4.1. BJT Differential Amplifier

Design this amplifier to meet the following specifications :

1. Single ended voltage gain = | 25 |
2. Transistor Quiescent Ic (DC) = 0.25 mA (Transistor type CA3046 Integrated Array)
3. Vcc = +6 volts
4. Vee = -6 volts

Before wiring any hardware, the amplifier should be designed using manufacturer's data and theory given below. You should check that the transistors are operating in the right region of their static characteristics and that no maximum rating is exceeded. The system should be simulated using PSPICE with the reduced hybrid model representing each transistor. Hybrid parameters are available in the manufacturer's data section or may be deduced from transistor static characteristic plots. For a successful design you should be very careful in determining the correct values of hie and hfe to use at the specified quiescent point.

The transistor is to be operated in the single ended mode so that the circuit should be as shown in Figure 4.3 in which the base of Q2 is grounded. The output can be taken from either collector but note that there will be 180° phase difference between the two outputs.

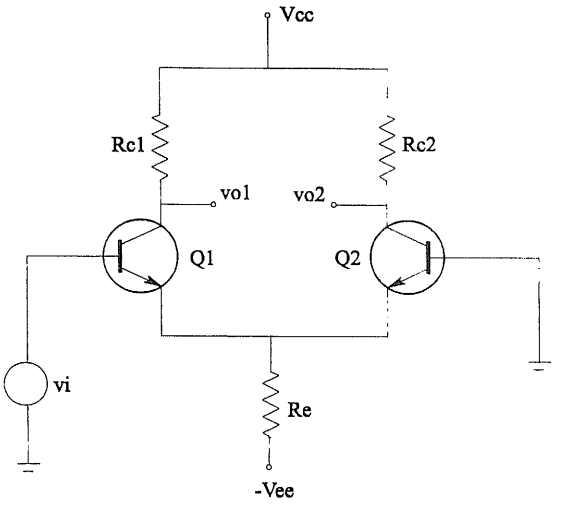

Figure 4.3 Single ended operation of differential amplifier

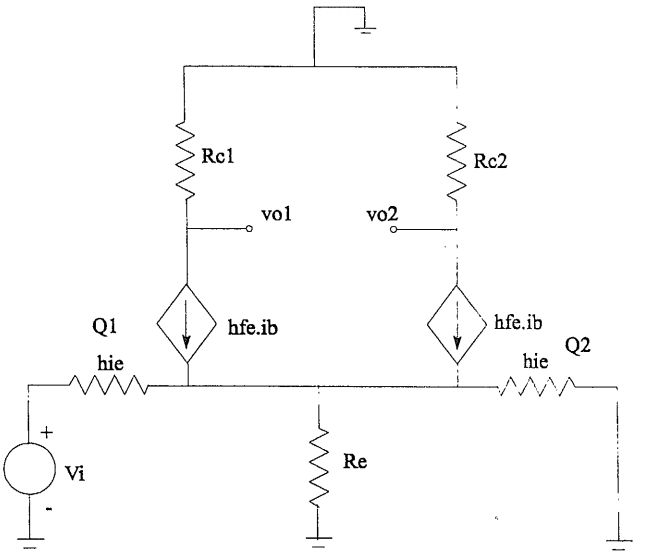

Figure 4.4 Single ended small signal model of differential pair

Part 2 - Amplifier Characteristics

For the PSPICE simulated amplifier which you have designed

(a) Determine the common mode gain and hence the common mode rejection ratio.
(b) Determine the input resistance of the simulation.
(c) Carry out measurements on your hardwired version to determine the above parameters.

THEORY

DC operation

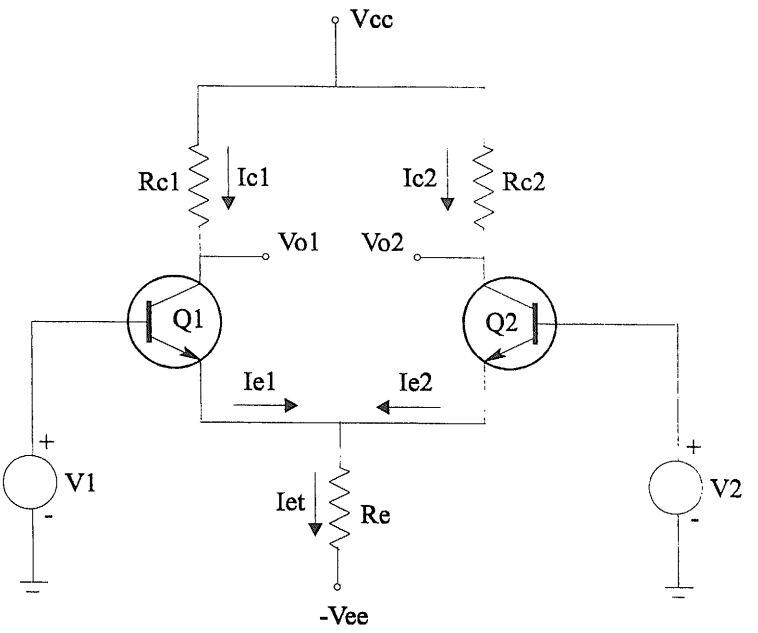

Figure 4.5 The differential pair

DC analysis begins by considering the voltage drops around the loops including the base/emitter junctions of either transistor Q1 or Q2 in the circuit of Figure 4.5. Since the voltage with respect to ground at each emitter is the same

$$V1 - VBE1 = V2 - VBE2 \tag{4.1}$$

Using the ideal diode equation and the Ebers Moll relationships recall that the IV characteristics for BJT base/emitter junction may in general be modelled by

$$I_C = I_O \exp\left(\frac{V_{BE}}{V_T}\right) \tag{4.2}$$

Since $I_c = \alpha I_{Et}$, (4.2) may be written

$$I_E = \frac{I_O}{\alpha} \exp\left(\frac{V_{BE}}{V_T}\right) \tag{4.3}$$

Rearranging (4.3) gives

$$V_{BE} = V_T \ln\left(\frac{\alpha I_E}{I_0}\right) \tag{4.4}$$

Using (4.4), equation (4.1) may be written as

$$V_1 - V_T \ln(\frac{\alpha I_{E1}}{I_{O1}}) = V_2 - V_T \ln(\frac{\alpha I_{E2}}{I_{O2}}) \tag{4.5}$$

Since the transistors used in differential amplifiers should be matched pairs, the Io's and α's should be identical and therefore rearrangement of (4.5) gives

$$\frac{I_{E1}}{I_{E2}} = \exp(\frac{V_1 - V_2}{V_T}) \tag{4.6}$$

From Figure 4.5 using KCL at the emitters

$$I_{E1} + I_{E2} = I_{Et} \tag{4.7}$$

Substituting from (4.7) into (4.6) twice for I_{E1} and I_{E2} yields

$$I_{E1} = \frac{I_{Et}}{1 + \exp[\frac{V_2 - V_1}{V_T}]} \tag{4.8}$$

and

$$I_{E2} = \frac{I_{Et}}{1 + \exp[\frac{V_1 - V_2}{V_T}]} \tag{4.9}$$

Equations (4.8) and (4.9) illustrate the fundamental operating conditions for the differential amplifier.

To summarize :

(a) The amplifier responds only to differential voltages $\pm (V_1 - V_2)$.

(b) If $V_1 = V_2$ both emitter currents are the same and equal to $\frac{I}{2}$

(c) Due to the exponential form of (4.8) and (4.9) a change of only a few hundred millivolts in $\pm (V_1 - V_2)$ is required to cut off or saturate one or other of the transistors.

Small Signal ac Operation

Analysis of the amplifying properties of the differential amplifier is achieved by replacing Q1 and Q2 by their small signal equivalent circuits. Since the configuration of each transistor is common emitter, the reduced hybrid model is appropriate for intermediate and low frequency operation. Note that since the circuit is direct coupled to an input source (no DC blocking capacitor) the small signal model is also appropriate for the analysis of DC amplification provided the transistors remain in the linear region and DC shifts are small. The resulting circuit is shown in Figure 4.6. We are interested primarily in differential mode amplification and seek by design to reduce common mode effects.

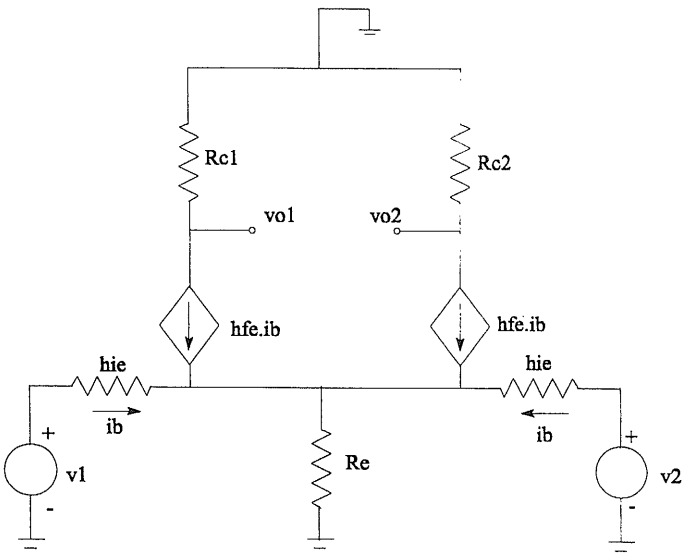

Figure 4.6 Small signal equivalent circuit

The two input voltages v1 and v2 may be written in terms of differential and common mode components as follows

$$v_{dmi} = v1 - v2 \tag{4.10}$$

where v_{dmi} is the differential voltage. The common mode voltage is usually taken as the average of the two input voltages v1 and v2.

$$v_{cmi} = \frac{v1 + v2}{2} \tag{4.11}$$

(4.10) and (4.11) may be rearranged giving v1 and v2 in terms of differential and common mode elements

$$v1 = \frac{v_{dmi}}{2} + v_{cmi} \tag{4.12}$$

and

$$v2 = -\frac{v_{dmi}}{2} + v_{cmi} \tag{4.13}$$

Since the small signal circuit shown in Figure 4.6 is a linear model, application of the superposition theorem allows us to consider separately the effects of differential and common mode components of (4.12) and (4.13).

Differential Gain

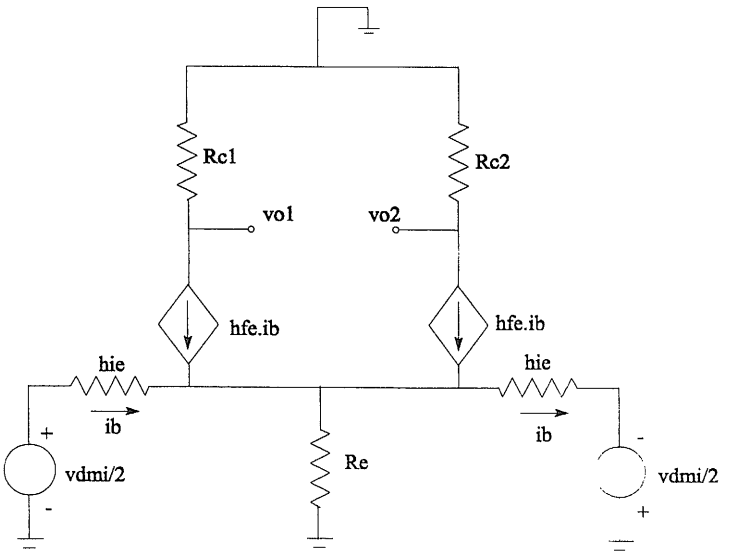

Figure 4.7 Differential mode small signal model

Summing the voltages round the loop including the inputs and bases

$$\frac{\text{vdmi}}{2} - \text{hie.ib} - \text{hie.ib} + \frac{\text{vdmi}}{2} = 0 \tag{4.14}$$

or

$$\text{Vdmi} = 2\text{hie.ib} \tag{4.15}$$

Therefore the single-ended gain is given by

$$Ad = \frac{vo1}{Vdmi} = -\frac{Rc.ic}{2hie.ib} = -\frac{hfe.Rc}{2hie} \tag{4.16}$$

and the double ended gain is given by

$$Add = \frac{vo1 - vo2}{vdmi} = 2Ad = -\frac{hfe.Rc}{hie} \tag{4.17}$$

Evaluating the voltage across Re for the left hand side of the circuit of Figure 4.7

$$\frac{Vdmi}{2} - hie.ib = Ve \tag{4.18}$$

and similarly evaluating voltage across Re for the right hand circuit of Figure 4.7

$$Ve = hie.ib - \frac{vdmi}{2} \tag{4.19}$$

Adding (4.18) and (4.19)

$$2ve = 0 \tag{4.20}$$

and therefore

$$ve = 0 \tag{4.21}$$

Note that we are concerned with ac or dc small signal parameters. Equation 4.21 implies no change in the DC quiescent voltage across Re.

Common Mode Gain

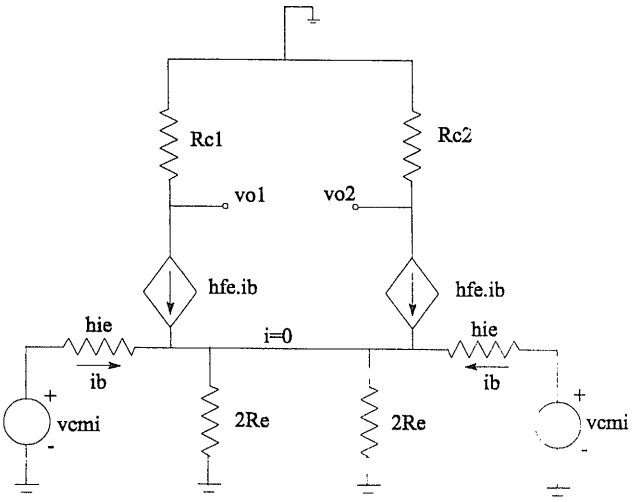

Figure 4.8 Common mode small signal model

For the common mode terms in (4.13) and (4.14) the small signal model of Figure 4.8 may be drawn. Separating Re into two parallel resistances each of twice the value of Re enables analysis to proceed on the basis of one side only of the circuit of Figure 4.8. Since the circuit is considered fully symmetrical, it follows immediately that the current between the resistances is zero. The single ended output voltage is given by

$$\text{vo1} = \text{Rc1.hfe.ic} \tag{4.22}$$

Writing KVL round the base/emitter loop

$$vcmi - hie.ib - ib(1 + hfe)2\,\text{Re} = 0 \tag{4.23}$$

Rearranging

$$vcmi = ib\{hie + (1 + hfe)2\,\text{Re}\} \tag{4.24}$$

The single ended gain is therefore

$$\frac{vo1}{vcmi} = -\frac{Rc1.hfe}{hie + (1 + hfe)2\,\text{Re}} \tag{4.25}$$

Since Re is usually chosen to be large and hfe >> 1 for most transistors of interest, this reduces to

$$\frac{vo1}{vcmi} = -\frac{Rc1}{2\,\mathrm{Re}} \tag{4.26}$$

For the general case operation of a true differential amplifer, common mode gain is considered extremely undesirable. To minimize it, Re should be chosen to be as high as possible. However it should be low enough to permit the appropriate DC quiescent quiescent current to flow. A more 'evolved' amplifier desgn replaces Ree with a constant current source which can be arranged to meet both of these criteria.

Common Mode Rejection Ratio

From (4.17) and (4.26) the ratio of the differential gain to common mode gain is easily deduced by division, ie

$$\frac{\text{Differential Mode Gain}}{\text{Common Mode Gain}} = \frac{hfe\ \mathrm{Re}}{hie} \tag{4.27}$$

This ratio is known as the common mode rejection ratio (C.M.R.R.) and because of the magnitudes involved it is usually expressed in logarithmic form

$$CMRR = 20\log[\frac{hfe\,\mathrm{Re}}{hie}] \tag{4.28}$$

Input Resistance

It was shown (4.21) that for differential operation the small signal voltage drop across Re is zero. Both transistor emitters appear at ground potential and therefore the input resistance viewed between the base and common of a single transistor is hie. For a differential signal between the bases of Q1 and Q2 the input resistance is double this

$$\mathrm{Ri(diff)} = 2\mathrm{hie} \tag{4.29}$$

For common mode signals the input resistance may be deduced by writing KVL around the loop including the base/emiiter junction of either transistor

$$vcmi - hieib - 2\,\mathrm{Re}(1 + hfe)ib = 0 \tag{4.30}$$

Rearranging

$$Ri(CommonMode) = \frac{vcmi}{ib} = hie + 2\,\mathrm{Re}(1 + hfe) \tag{4.31}$$

Usually hfe and Re dominate in this equation so that the common mode input resistance may be closely approximated by

$$Ri(CommonMode) = 2\,\mathrm{Re}hfe \tag{4.32}$$

EE LABORATORY IV

ECE312

Experiment 5. RC Sinusoidal Oscillators

PURPOSE :

This laboratory provides an introduction to the background, analysis and design of sinusoidal oscillators using RC feedback networks and active devices to achieve the criteria for continuous oscillations to occur.

EQUIPMENT REQUIRED :

1 Operational amplifier μA741
1 CEU development station
Resistors and capacitors as required

INTRODUCTION :

An understanding of the factors that influence stability is fundamental to the successful design of many electronic systems. The engineer may need to minimize the time for a position control system to reach a particular condition or possibly frequency response tailoring of a high order active filter is required. In either case optimization may lead to marginal stability with the possibility of transfer function poles becoming dangerously near transition into the right hand side of the complex plane. In the design of an oscillator the promotion of marginal instability is a design requirement.

A useful way to view oscillator principles is to the use a mechanical analogy and consider the motion of a pendulum. This is a second order system with energy stored in the form of potential and kinetic energy. In motion, energy is continuously traded between these two forms while being dissipated through frictional losses. If no energy is injected into the system it will ultimately come to rest. To keep the pendulum swinging, injection of energy is required. However if too little energy is injected, the motion will decay : too much energy and the amplitude of successive swings will increase resulting in instability. A major goal of design is to arrange for injection of energy to exactly counterbalance the losses. Whether one is considering a mechanical, electrical or any other type of oscillating system this is a fundamental concept which may be stated as follows

$$\sum(\text{System gains}) = \sum(\text{System losses}) \tag{5.1}$$

To keep the pendulum in motion, input of energy must be accomplished in a particular way. Clearly the energy injection needs to assist the pendulum motion rather than impede it. If a feedback loop is used to detect the motion and provide the correct input this requirement may be summarized as :

$$\sum(\text{System loop phase angles}) = 360^{\circ} \tag{5.2}$$

Equations (5.1) and (5.2) are the Barkhausen criteria which are stated in a more formal way at the beginning of the theory section.

In the theoretical design of a linear electronic oscillator an immediate difficulty arises. How do we tread the infinitely narrow path suggested by (5.1). Too much gain and the output amplitudes successively increase. Too little gain and the system will not start oscillating at all. With too little gain oscillation may start with the input of noise. However with inadequate "energy injection" the oscillation rapidly decays to a quiescent DC value. The practical answer to this problem is that usually the gain is arranged to be a little greater than would be suggested by (5.1) so that the oscillator behaves like a pendulum with too much energy injection. In the electronic case either saturation limits the oscillation amplitude or alternatively a non-linear element is deliberately introduced to limit the amplitude.

In this laboratory you will be asked to design two sinusoidal oscillators and select the gain factors so that the amplitudes only just enter saturation. If the gain is too large your sinusoidal oscillators will actually become square wave generators. You should be a little cautious when you use PSPICE to simulate your design and realize that you are designing for a gain which is a little high. Your PSPICE model transient response should show increasing oscillations. The rate at which the amplitude of these oscillations should increase in the simulation is a matter for you to decide when you compare your SPICE results with the "real thing."

PROCEDURE

Part 1 - Phase shift oscillator design using an OP AMP

Using the theory section design a phase shift oscillator to produce as output a voltage sine wave . Using preferred component values (R and C) in your design and a μA741 operational amplifier you are to meet the following specifications :

Sinusoid Amplitude	6.0 volts ± 0.5 volts (peak to peak)
Frequency	1 kHz ± 10%
Output resistance	50 ohms ± 5 ohms

The oscillator should be designed theoretically and simulated using SPICE before implemented in hardware. "Slight adjustment "of component values may be necessary at the hardware stage to achieve a totally satisfactory design.

Part 2 - Wien Bridge oscillator design using BJT amplification

Using the same specification as in Part 1 design a Wien Bridge oscillator using the μA741 operational amplifier as the amplifying element. As above the theoretical design should be supported by SPICE simulation prior to hardware implementation.

THEORY

The standard block diagram for a single loop feedback system is given below :-

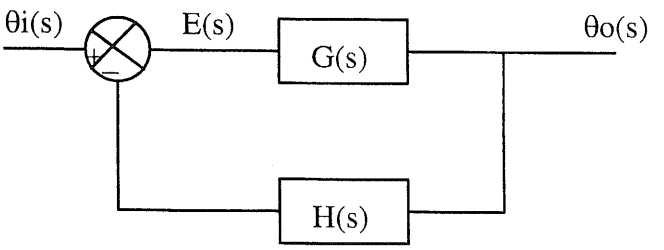

Figure 5.1

Writing the input/output relationship for the above circuit in transfer function form

$$\frac{\theta_0(s)}{\theta_i(s)} = \frac{G(s)}{1+G(s)Hs)} \tag{5.3}$$

For instability to occur the Barkhausen criteria criteria must be satisfied and for sinusoidal oscillation we are concerned with operation in the real frequency domain where $s = j\omega$ and

$$\angle G(j\omega)H(j\omega) = 180° \tag{5.4}$$

and

$$|G(j\omega)H(j\omega)| = 1 \tag{5.5}$$

Equation (5.4) implies a complete loop phase shift of 360 degrees for oscillation to take place **since an additional 180° phase shift occurs across the summing element shown in the block diagram of Figure 5.1** (note the negative sign). Also equation (5.5) requires a complete loop gain of 1. In practice gains higher than this will be employed leading to the possibility of saturation and consequently waveform distortion.

THE PHASE SHIFT OSCILLATOR

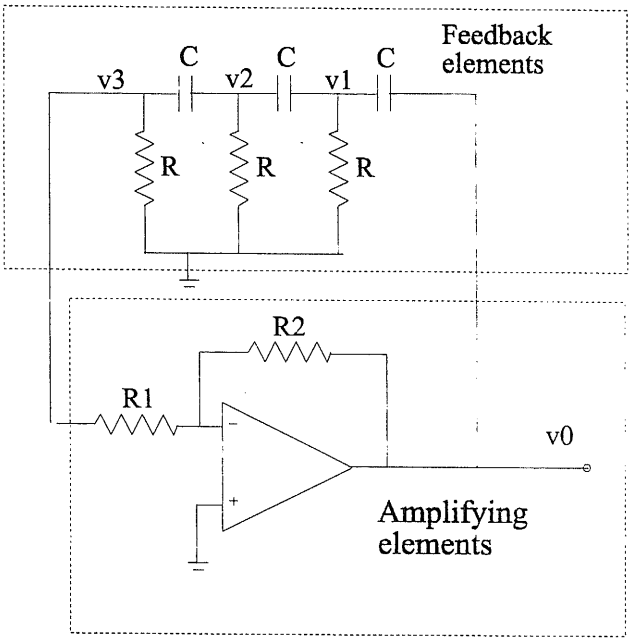

Figure 5.2. The phase shift oscillator using an operational amplifier as active element

ANALYSIS OF THE PHASE SHIFT FEEDBACK NETWORK

Extracting the feedback network from the circuit of Figure 5.2 gives

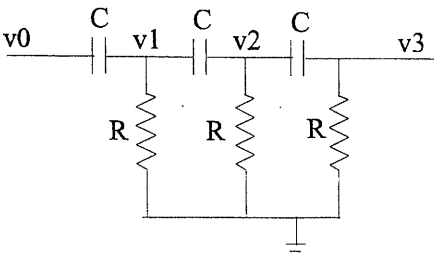

Figure 5.3 Phase shift network

To design an oscillator using the above phase shift network in the feedback path we require the phase shift to be 180°. We therefore need to examine the input/output relationship and begin by writing nodal equations. In writing these equations it is assumed that the output is unloaded. In the complete circuit of Figure 5.2 this assumption is only valid if R1 is relatively large. The nodal equations are

$$[v0 - v1]sC = \frac{v1}{R} + [v1 - v2]sC \tag{5.6}$$

$$[v1 - v2]sC = \frac{v2}{R} + [v2 - v3]sC \tag{5.7}$$

Also

$$[v2 - v3]sC = \frac{v3}{R} \tag{5.8}$$

Rearranging (5.6), (5.7), (5.8)

$$v0sC = v1\left[\frac{1}{R} + 2sC\right] - v2sC \tag{5.9}$$

$$v2sC = v3\left[\frac{1}{R} + sC\right] \tag{5.10}$$

$$v3sc = -v1sC + v2\left[\frac{i}{R} + 2sC\right] \tag{5.11}$$

Equations (5.9), (5.10) and (5.11) may be solved by elimination and back substitution giving the following transfer function

$$\frac{v3(s)}{v0(s)} = \frac{-(sC)^2}{\left[\frac{1}{R}+2sC\right]sC - \frac{1}{sC}\left[\frac{1}{R}+sC\right]^2\left[\frac{1}{R}+3sC\right]} \tag{5.12}$$

Replacing s by jω enables (5.12) to be rewritten as a frequency response function. After manipulation (5.12) becomes

$$\frac{v3(j\omega)}{v0(j\omega(\,)} = \frac{\omega^3\tau^3}{\left[\omega^3\tau^3 - 5\omega\tau\right] - j\left[1-6\omega^2\tau^2\right]} \tag{5.13}$$

The phase is given by

$$\phi = \tan^{-1}\left[\frac{1-6\omega^2\tau^2}{\omega^3\tau^3 - 5\omega\tau}\right] \tag{5.14}$$

Since ϕ must be 180° and tan 180°= 0 it follows from (5.14) that

$$1-6\omega^2\tau^2 = 0$$

or in terms of frequency (Hz)

$$f = \frac{1}{2\pi\tau\sqrt{6}} \tag{5.15}$$

The second requirement for oscillation is that the complete loop gain must be 1. Therefore attenuation through the feedback network must be balanced by appropriate design of the amplifier gain.
The attenuation through the feedback network is given by the magnitude of the complex number, equation (5.13). Substituting the frequency from (5.15) yields

$$\left|\frac{v0(j\omega)}{v3(j\omega)}\right| = \frac{\left[\sqrt{6}\right]^3}{\left[\left[\left[\frac{1}{\sqrt{6}}\right]^3 - \frac{5}{\sqrt{6}}\right]^2 + \left[1-\frac{1}{6}\right]^2\right]^{0.5}} \tag{5.16}$$

or

$$\left|\frac{vo}{v3}\right| = \frac{1}{29} \tag{5.17}$$

Therefore the amplifier gain must be greater than 29 for oscillation to be sustained.

THE WIEN-BRIDGE OSCILLATOR

The phase shift and amplifier block diagram for this oscillator is shown in Figure 5.4

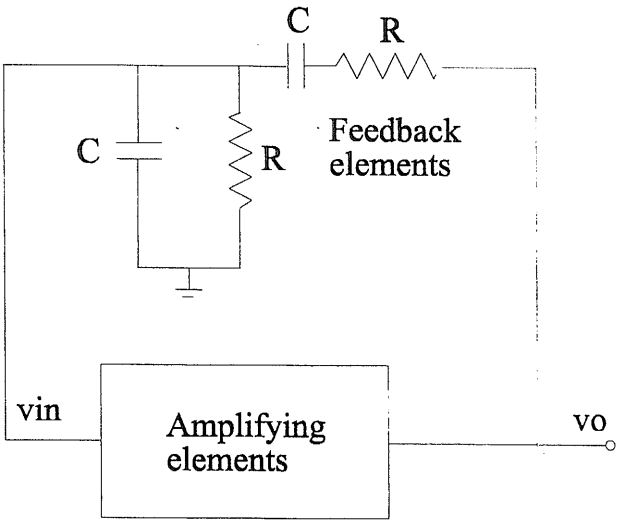

Figure 5.4 The Wien-Bridge oscillator

The circuit consisting of the feedback elements in figure 5.4 consists of phase lag and phase lead stages. If we can design the feedback circuit so that exact phase cancellation of the lead and lag terms occurs and further arrange that the phase shift provided by the feedforward amplifiying circuit is 360°, a complete loop phase shift of 360° will have been achieved. This meets the phase requirement of the Barkhausen criteria for oscillation indicated in (5.4).

Writing the transfer function for the feedback circuit from the right hand side to the left

$$\frac{vin(s)}{vo(s)} = \frac{vin(s)}{vo(s)} = \frac{\dfrac{R/sC}{R+1/sC}}{R+1/sC+\dfrac{R/sC}{R+1/sC}} \tag{5.18}$$

Mutiplying numerator and denominator by $(R+1/sC)$ gives

$$\frac{vin(s)}{vo(s)} = \frac{R/sC}{(R+1/sC)^2+R/sC} \tag{5.19}$$

Expanding the squared term and multiplying the numerator and denominator by sC gives

$$\frac{vin(s)}{vo(s)} = \frac{R}{3R + (R^2sC + 1/sC)} \tag{5.20}$$

Replacing s by jω yields

$$\frac{vin(j\omega)}{vo(j\omega)} = \frac{R}{3R + (j\omega R^2C + 1/j\omega C)} \tag{5.21}$$

If the phase of this complex number is to be zero the imaginary terms in the denominator must cancel leaving only a real component, i.e.

$$\omega R^2C = 1/\omega C \tag{5.22}$$

or

$$\omega = \frac{1}{RC}$$

In terms of Hz rather than rads/sec

$$f = \frac{1}{2\pi RC} \tag{5.23}$$

With the imaginary terms of (5.21) summing to zero the attenuation provided by this circuit is determined as

$$\frac{vin(\omega)}{vo(\omega)} = \frac{R}{3R} = \frac{1}{3} \tag{5.24}$$

Therefore for the the total circuit to meet the second Barkhausen criterion (5.3) the gain of the amplifying feed forward element should be 3.

EE LABORATORY IV

ECE 312

Experiment 6. Theshold Detection

PURPOSE:

This laboratory addresses a common problem which is the detection of a threshold voltage level where the signal of interest might be required to trigger alarm circuitry or detect a specific level in noise. A level detection problem is presented in the form of several required waveforms and you are asked to design an integrator and Schmitt trigger circuit as part of a system to implement these waveforms.

INTRODUCTION :

In instrumentation and control applications it is often necessary to detect a specified threshold level of a relatively slowly changing voltage waveform. Examples are the output of an aircraft radio altimeter forming part of the aircraft ground proximity detection system or the output of an industrial fire detection alarm system detecting ambient temperature. Such systems are critical and as such, reliable detection is of paramount importance. The superposition of low level or impulsive noise on a slowly varying DC output voltage waveform may lead to problems in detecting a specific threshold level cleanly . Such a signal is indicated in Figure 6.1. This shows a slowly moving waveform with "glitches" due to the presence of noise. One "glitch" is shown occurring at time to. This glitch happens as the voltage waveform nears the threshold level Vr when detection and switching action should take place.

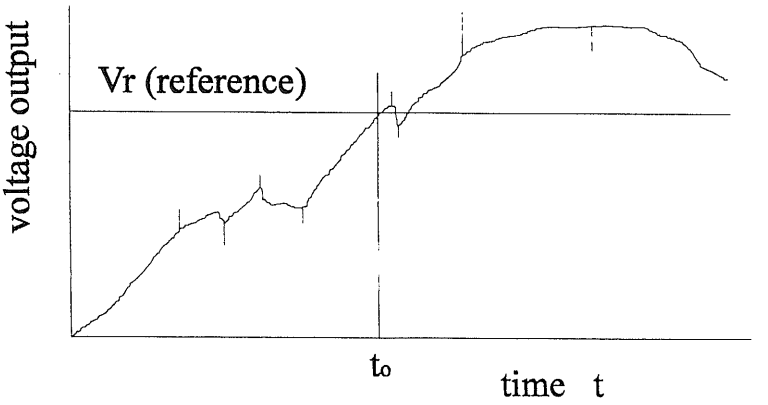

Figure 6.1 Slowly moving waveform with superimposed noise

A simple method of detecting a voltage threshold is shown in Figure 6.2 This is a high gain operational amplifier connected in the open loop mode as a comparator with the reference voltage Vr derived from a stable DC voltage supply and set by means of a potentiometer formed by R1 and R2.

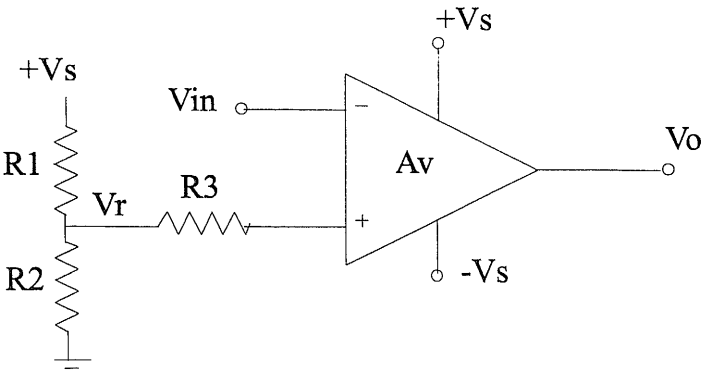

Figure 6.2 Simple comparator circuit

If the simple comparator circuit is used to detect the crossing of the threshold level indicated in Figure 6.1 noise may cause multiple comparator switching. This can be a problem in that data processing equipment supplied by the comparator output may generate race conditions and could misread. A second problem which can result is that systems brought on line by threshold detection may cause the power supply voltage to fluctuate and reset the comparator. This problem is particularly likely in a case where heavy current switching takes place. An example from the author' s past is the case of several large control valves being activated by the output of a carbon dioxide monitor in a process. As the control valves moved the power supply voltage dipped by more than 10% which reset the monitor threshold detector. The statement that instability resulted only mildly describes the noise and chaos which broke out !
A solution to this problem is to design a comparator with thresholds which are different for positive and negative going inputs with a transfer characteristic as shown in Figure 6.3.

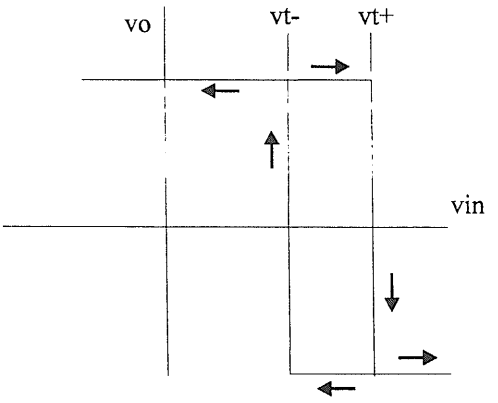

Figure 6.3 Comparator transfer characteristics with hysteresis

As vin increases from zero no switching occurs until the upper threshold voltage Vt^+ is reached at which point the output switches from positive to negative. As vin then decreases from above Vt^+ towards zero, switching for this negative going signal occurs at Vt^-. Thus a form of hysteresis has been introduced and the secret of successful practical design is to make sure that the hysteresis window ($Vt^+ - Vt^-$) is greater than the noise on the system.
A circuit which will generate the required hysteresis is the Schmitt trigger circuit indicated in Figure 6.4

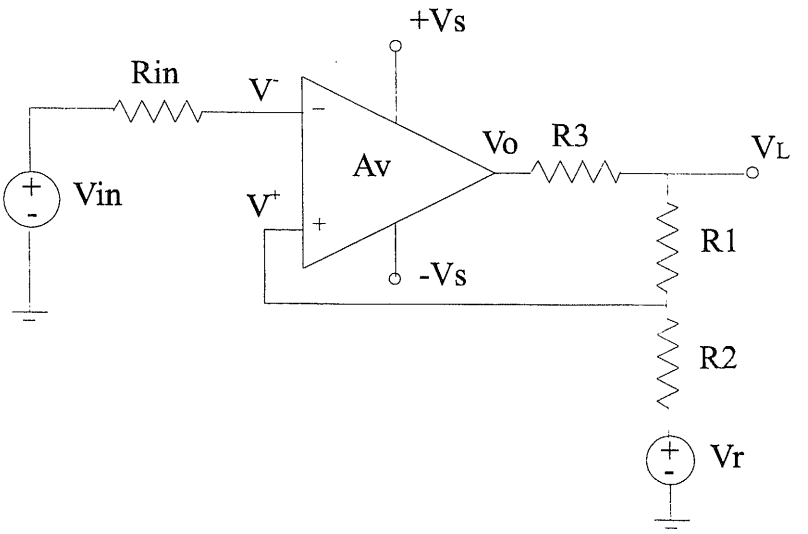

Figure 6.4 The Schmitt trigger circuit

PROCEDURE

You are asked to consider the waveforms shown in Figure 6.5. on the next page. Design a system which will generate all three of these waveforms. You may use software to generate the upper square wave shown in Figure 6.5 if you wish but the triangular and lower pulse waveform should be generated using an integrator and Schmitt trigger circuit. Any combination of devicesthat can achieve the specifications is acceptable. The component values required to complete the design should be obtained through study of the theory section, thought, and calculation.

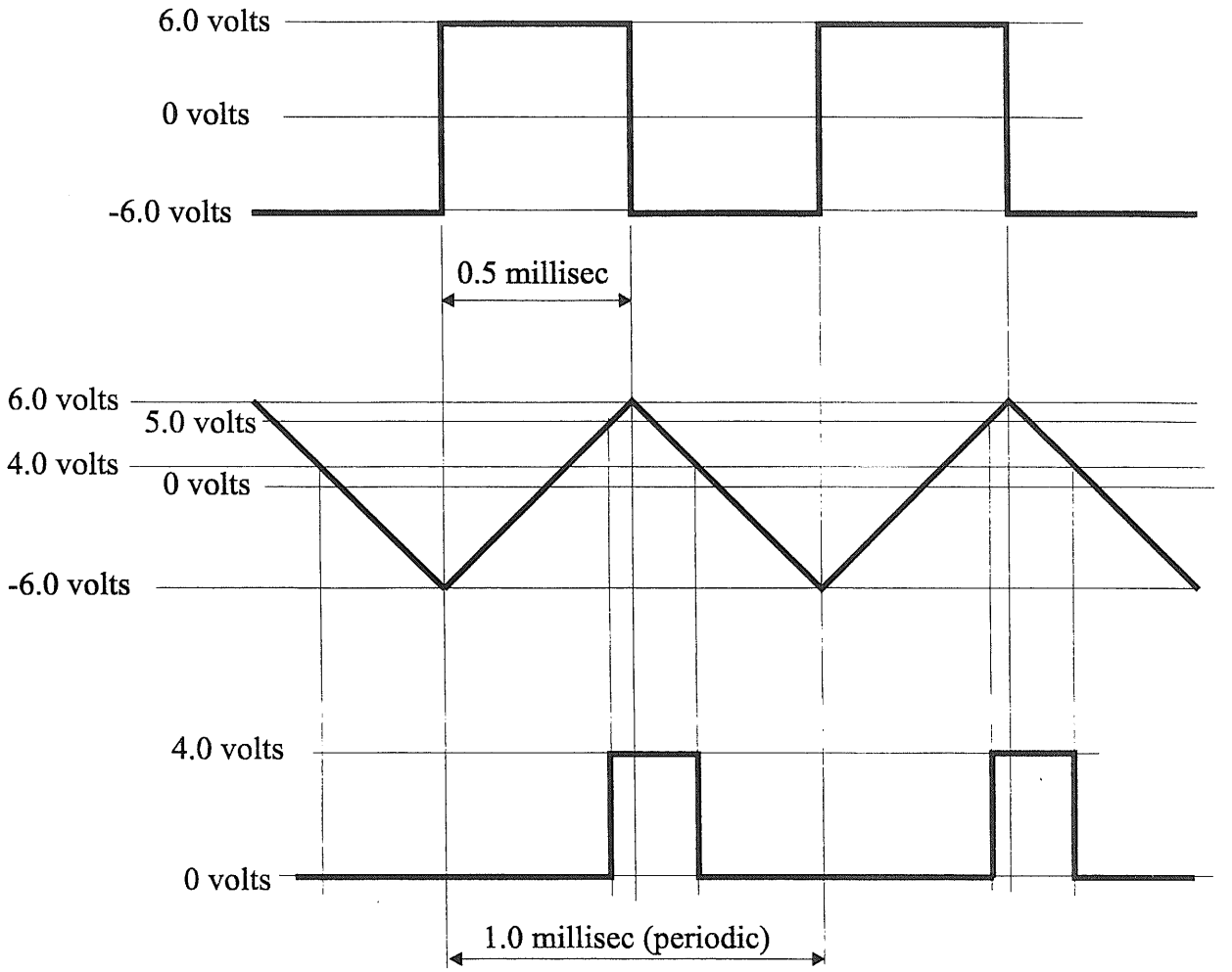

Figure 6.5 Waveform design requirements

Additional Design Constraints

1. Amplifer power supply should be Vs = ± ≤ (6 - 10) volts
2. System output resistance = 50 Ω ± 10%
   {Note that R3 shown in Figure 6.5 is the internal amplifer output resistance)
3. The output voltage waveform should be within ±0.5 volts of the limits (4, 0 volts) shown in Figure 6.5

The circuit should be designed, simulated and finally implemented in hardware.

THEORY

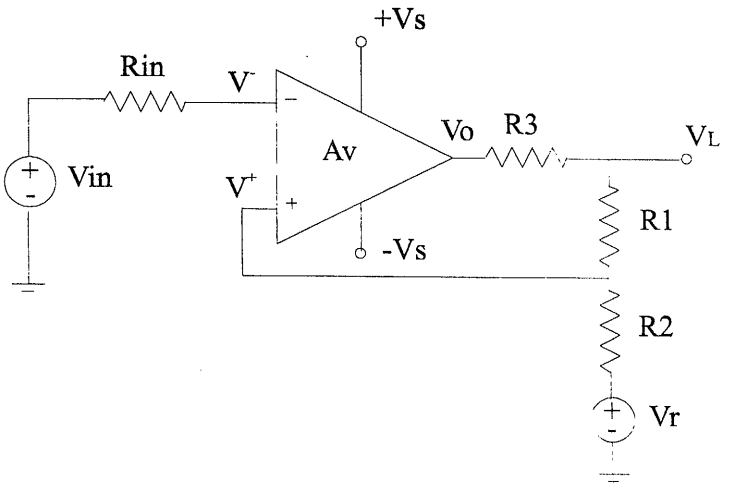

Figure 6.6 Schmitt trigger circuit

Analysis begins by noting that

$$vin = v^- \tag{6.1}$$

and starting from the condition that

$$v^- < v^+ \tag{6.2}$$

Since the operational amplifier is operating in the open loop condition the gain is extremely high.
Applying the basic input/output relationship for the operational amplifier

$$vo = A(v^+ - v^-) \tag{6.3}$$

yields for the condition (6.2) above

$$vo = +Vo \tag{6.4}$$

where +Vo is the positive operational amplifier saturation voltage (unloaded).

Note that the output resistors R1 and R2 in conjunction with R3 (internal OP AMP output resistance) result in voltage division of Vo. V_L is the measurable output voltage.

Let Vt^+ = the input threshold voltage (at the non-inverting input) for a positive going input vin. To determine Vt^+ the following subcircuit may be drawn

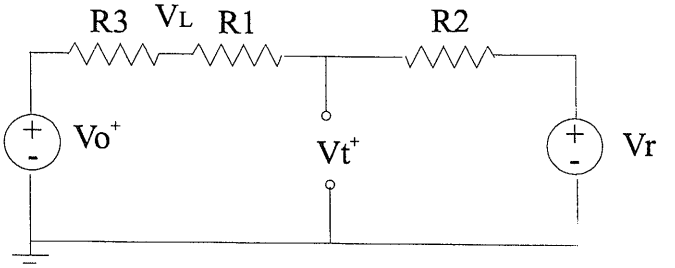

Figure 6.5 Subcircuit to aid in determining Vt^+

Using superposition

$$Vt^+ = \frac{Vo^+ R2}{(R1+R2+R3)} + \frac{Vr(R1+R3)}{(R1+R2+R3)} \tag{6.5}$$

Therefore if vin is increased in the positive direction from zero the output remains at +Vo until Vt+ is reached and then switches rapidly to -Vo.
For negative going input signals vs starting above Vt+ a similar subcircuit may be drawn and Vt^- determined

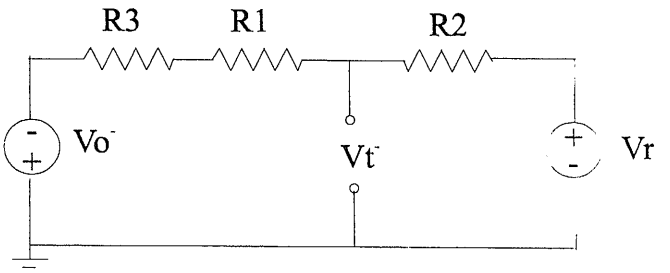

Figure 6.6 Subcircuit to aid in determining Vt^-

Applying superposition once again

$$Vt^- = \frac{-VoR2}{(R1+R2+R3)} + \frac{Vr(R1+R3)}{(R1+R2+R3)} \tag{6.6}$$

The width of the "hysteresis loop" is given by the difference between the threshold values ie

$$\Delta V = Vt^+ - Vt^- \tag{6.7}$$

From (6.5), (6.6) and (6.7)

$$\Delta V = \frac{2R2Vo}{(R1+R2+R3)} \tag{6.8}$$

The window width ΔV is as indicated in Figure 6.7 below

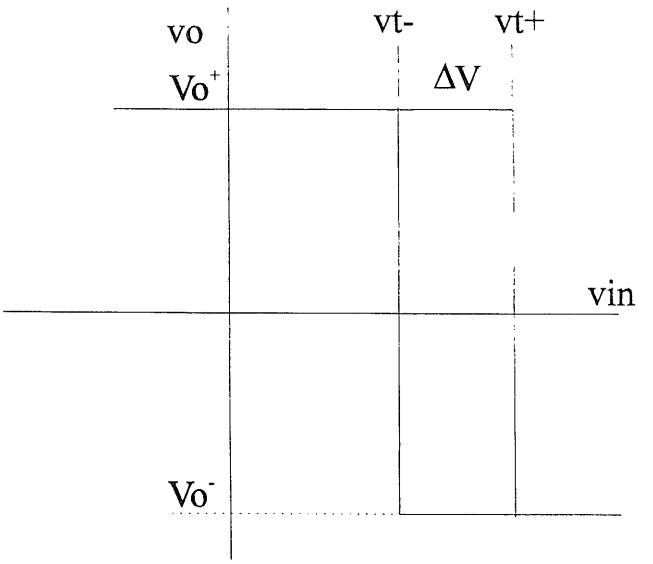

Figure 6.7 The hysteresis Window identifying ΔV

Appendix B

Useful Derivations

COMPLEX NUMBERS

A complex number may be represented in equation form in three different ways

(i) $z = a+jb$

(ii) $z = r(\cos \phi+j\sin \phi)$

(iii) $z = re^{j\phi}$

The above relationships may all be illustrated by the Argand diagram

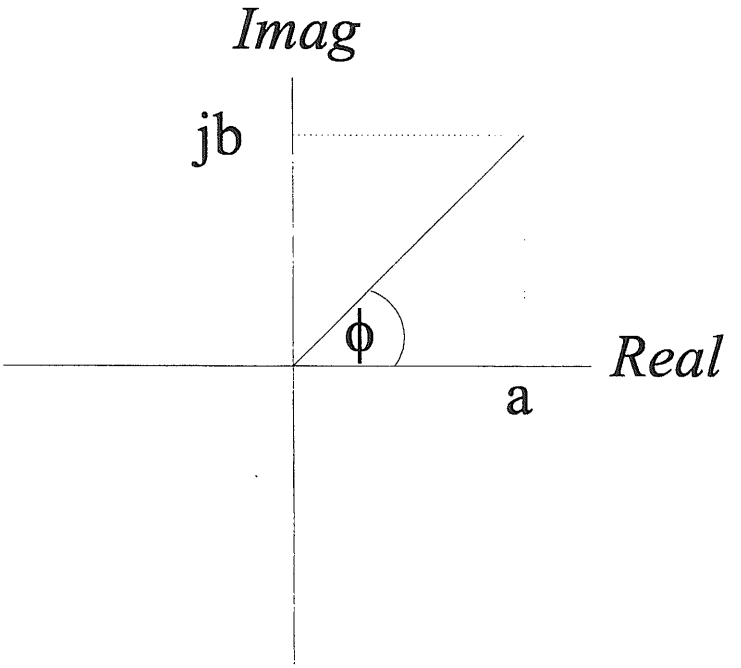

Figure 1. The Argand Diagram

Complex notation is therefore a neat way to describe and organize what amounts essentially to a two dimensional vector where the operator j maintains the orthogonality (90°) between the quantities indicated by the somewhat mystical terms ***Real*** and ***Imaginary***.
From the Argand diagram using right angle triangular relationships, the ***phase*** ϕ is given by

$$\phi = \tan^{-1}\frac{b}{a} = \sin^{-1}\frac{b}{r} = \cos^{-1}\frac{a}{r}$$

and the ***Modulus*** or ***Magnitude*** r by

$$r = \sqrt{a^2 + b^2}$$

Note the following relationships if the **real** part is zero

$z = 0 + jb, \qquad \phi = \tan^{-1}\infty = 90°$

$z = 0 - jb, \qquad \phi = \tan^{-1(-}\infty) = -90°$

Therefore:-

Multiplying a number by j shifts its phase by +90°.
Multiplying a number by -j shifts its phase by -90°.

Also note:-

Multiplying a number by j twice or j^2 (= -1) shifts its phase by 180°.

A further manipulation which sometimes causes confusion is:-

$$\frac{1}{j} = \frac{j}{j^2} = -j$$

Addition or subtraction of complex numbers

This is usually best dealt with in the Cartesian form ((i) above).

$$(a1+jb1) \pm (a2+jb2) = (a1 \pm a2) \pm j(b1 \pm b2)$$

ie., the real and imaginary parts are added or subtracted separately.

Multiplication or division of complex numbers

To multiply or divide complex numbers the exponential form of (iii) proves the easiest to follow

If two complex numbers are represented by

$$z1 = r1e^{j\phi 1}$$

and

$$z2 = r2e^{j\phi 2}$$

the product is

$$z1*z2 = (r1*r2)e^{j(\phi1+\phi2)}$$

Note that in multiplication the Modulus (or magnitude) is given by the product of the magnitudes of z1 and z2 and the phase by the sum of the phases of z1 and z2.

Dividing the number z1 by z2 yields

$$\frac{z1}{z2} = \left(\frac{r1}{r2}\right)e^{j(\phi1-\phi2)}$$

Thus in the process of division the resulting modulus is the quotient of the moduli of z1 and z2 while the phase is given by the difference of the phases of z1 and z2.

Common manipulations with complex numbers

In engineering one is often faced with the need to find the magnitude and phase of a complex term such as

$$z = \frac{K}{a + jb} \quad \text{or} \quad z = \frac{\pm jc}{a + jb}$$

In both cases the simplest approach is to recognize these as quotients and apply the above results for quotients. Do not allow the fact that they are in Cartesian rather than exponential form to cause you confusion.

For the first of the two complex numbers $z = \frac{K}{a + jb}$, the magnitude and phase are deduced directly as follows

$$Magnitude = \frac{K}{\sqrt{a^2 + b^2}}, \qquad Phase = 0^\circ - \tan^{-1}\frac{b}{a}$$

For the second complex number $z = \frac{\pm jc}{a + jb}$ the magnitude and phase are obtained as

$$Magnitude = \frac{c}{\sqrt{a^2 + b^2}}, \qquad Phase = \pm 90^\circ - \tan^{-1}\frac{b}{a}$$

Appendix C

Laboratory Administration

ECE 312 **Electrical Engineering Laboratory IV** Aug. 1999

SYLLABUS

COURSE GOALS

Design and characterization of functional electronic circuits using solid-state devices
Use of simulation as a tool to aid in the design and testing of circuits.
Introduction to the use of virtual instrumentation via LabView.
Construction and measurement of circuit variables to validate design using an integrated laboratory test system.
The development of sound laboratory practices, data gathering, log keeping and written reporting skills.

PRE-REQUISITES

Courses ECE 320, ECE 311

Topics Basic circuit theory and analysis, mid-frequency discrete BJT and FET amplifier analysis and design .

REQUIRED MATERIALS

Course Reference Electronic Circuit Analysis and Design - Donald Neamen

Handbook ECE 312 Laboratory Manual

Lab Notebook Spriral or clothbound 8.1/2" × 11" notebook (required)

COURSE OUTLINE

Design experiments

Ex 1 BJT small signal parameters - revision of ECE 320 material and familiarization with integrated electronic test station (*short form lab. report*)

Ex 2 Operational Amplifiers - introduction to the design of systems using OP Amp's as building blocks (***full formal lab. report***)

Ex 3 Active current sources - the design of several types of active current sources - devices commonly used within the bias structure of integrated systems - (*short form lab. report*)

Ex 4 Differential Amplifiers - the design of bipolar circuits which are charactreristic of the inputs of Operational Amplifiers - (***full formal lab. report***)

Ex 5 Sinusoidal Oscillators - the design of different types of sinusoidal oscillator from basic principles of feedback (***full formal lab report***)

Ex 6 Level detection - introduction to a common problem in instrumentation - how to effectively sense a dc voltage level in what might be an electrically noisy environment - (*Short form lab report)*

LABORATORY FINAL

REPORTING REQUIREMENTS

Lab Notebook

All experiments require design effort. Consequently pre-lab thought and analysis are vitally important. You are required to maintain a laboratory notebook to record your design analysis and data gathered for experiments 1 to 6. Your notebook will be examined each week and assessed for neatness, clarity of exposition, design procedure and in-laboratory working log and analysis. This material will be graded and written feedback provided.

Full formal Laboratory Report

A formal report for each lab Ex's 2, 4 and 5 is due one week after completion of the experimental work or design validation, and must be typed on a **word processor.** Each report should contain about 4-6 pages of text. Each report must cover as a minimum the following topics:-

What was to be done
What were the design criteria/constraints
Design Analysis
Circuit of the design
A Spice Netlist/Scheme and Spice output information where appropriate
What was built, and how did it work
What problems were encountered, and how were they rectified
What would you do next time if faced with the same challenge
How does the circuit compare with the Spice results

The reoprt should start with an Abstract not to exceed 100 words which summarizes the work and which should be aimed at informing "Management" of what you are doing. Often in Industry this may constitute the most important section of the whole document.

Short Form Laboratory Report

Length

The maximum length of the report should be no more than 2 pages of text or analysis with possible additional pages containing drawings, software or other programing material where appropriate, or data in tabular form.

Required information as a header (short form report)

(a) Name and that of your laboratory partner
(b) Date that the laboratory work was performed
(c) Laboratory number and title

Content

(a) Goal
(b) Design calculations where appropriate
(c) Observations/conclusions

Both formal and short form reports will be graded and written feedback provided. Unsatisfactory reports will be returned to the student with a requirement that they be corrected and resubmitted. The report is to be written on the basis that the audience is technically trained.